RAiO

RA0086A

80 CH Segment/Common Driver

For Dot Matrix LCD

Specification

Version 1.2

February 21, 2020

RAiO Technology Inc.

Update History		
Version	**Date**	**Description**
1.0	October 04, 2010	Preliminary version
1.1	August 14, 2012	1. Update Section 7-2 : Die Form 2. Update Section 7-3 : Pad Coordinate
	August 8, 2013	1. Add Note on Figure 7-2
1.2	February 21 2020	1.Update Figure 5-5、Figure 5-7 2.Update Section 6-2

Chapter Content Page

1. Introduction

The RA0086A is an 80 channels LCD driver LSI which is fabricated by low power CMOS high voltage process technology. It can be used either as a COMMON driver or as a SEGMENT driver, by connecting its CS input to VDD or VSS. In segment driver mode, it can be interfaced in 1-bit serial or 4-bit parallel method by the controller. In common driver mode, dual type mode is applicable. And in segment mode application, the power down function reduces power consumption.

2. Features

- Power supply voltage: + 5V±10 %, + 3V± 10%
- Supply voltage for display: 6 to 30V (V_{DD}-V_{EE})
- In 80-SEGMENT driver or 80-COMMON driver selection, to set CS-pin voltage is VSS or VDD
- 4-bit parallel / 1-bit serial data processing (in segment mode)
- Single mode / dual mode operation (in common mode)
- Power down function (in segment mode)
- Applicable LCD duty: 1/64 – 1/256
- Interface

DRIVERS	
COM(Cascade)	SEG(Cascade)
RA0086A	RA0086A

- High voltage CMOS process
- Available package Type: LQFP-100 pin, Die

3. Pin Configuration

3-1 Internal Block Diagram

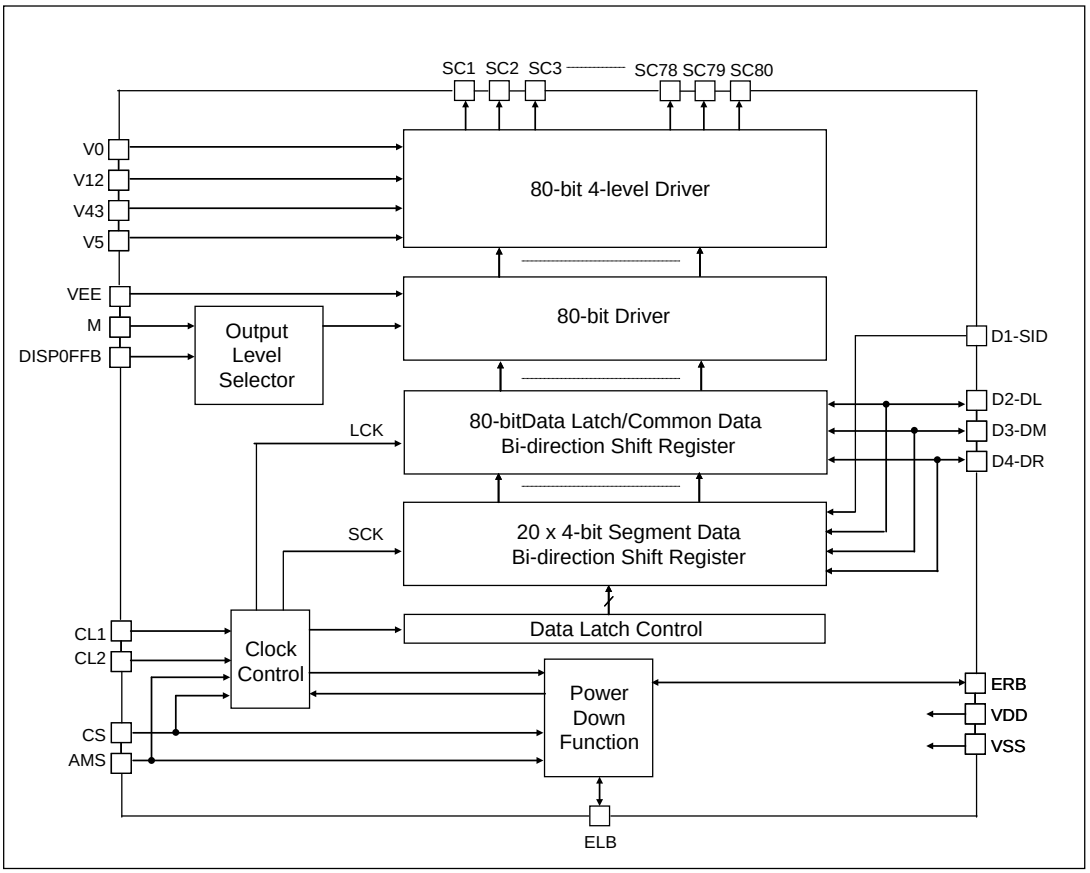


Figure 3-1 : Internal Block Diagram

3-2 Pin Assignment

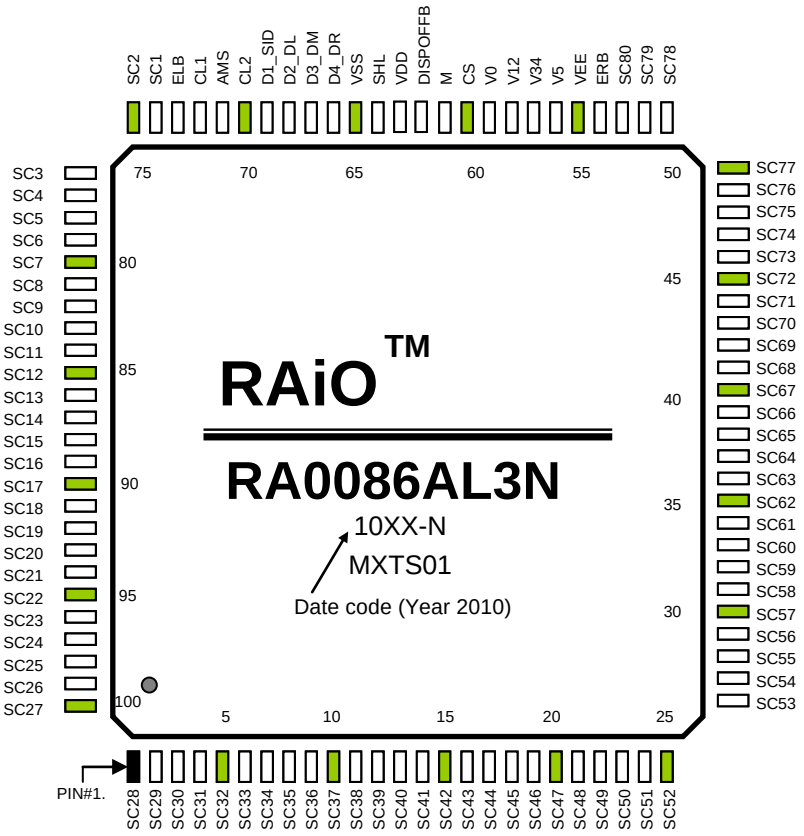


Figure 3-2 : LQFP-100 Pin Assignment

3-3 System Block Diagram

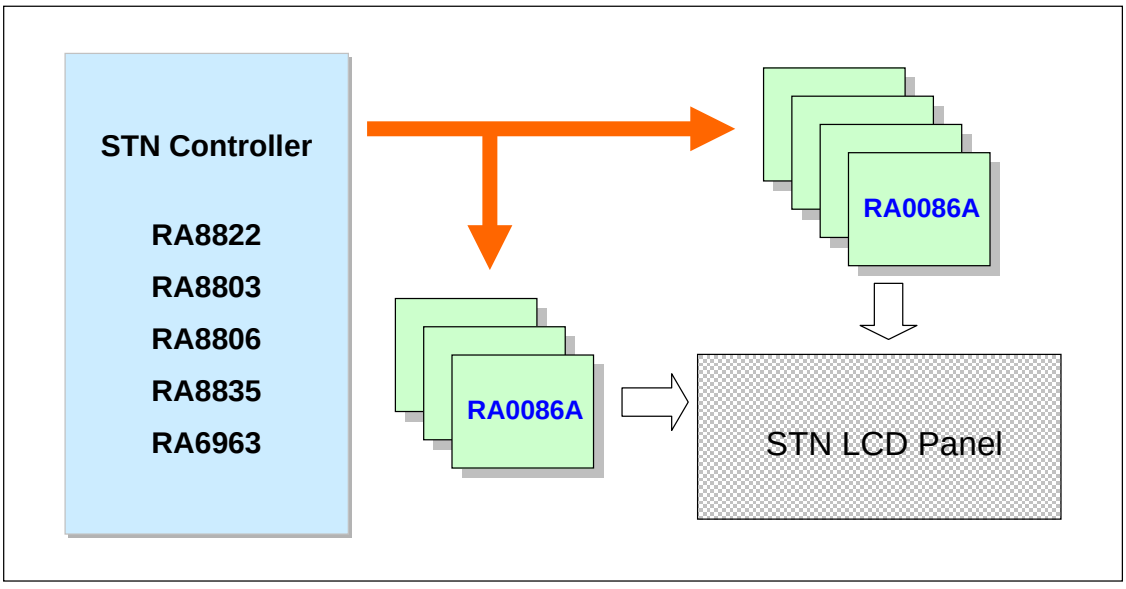


Figure 3-3 : System Block Diagram

4. Signal Description

4-1 Block Description

Name	Function	COM / SEG
Clock control	Generates latch clock (LCK), shift clock (SCK) and control clock timing according to the input of CL1, CL2 and control inputs (CS, AMS). In common driver application mode, this block generates the shift clock (LCK) for the common data Bi-directional shift register.	COM / SEG
Data latch control	Determines the direction of segment data shift, and input data of each Bi-directional shift register. In 4-bit segment data parallel transfer mode, data is shifted by a 4-bit unit. In common driver application mode, data is transferred to the common data shift register directly, which disables this block.	SEG
Power down function	Controls the clock enable state of the current driver according to the input value of enable pin (ELB or ERB). If enable input value is “Low”, every clock of the current driver is enabled and the clock control block works. But if enable input is “High”, current driver is disabled and the input data value has no effect on the output level. So power consumption can be lowered.	SEG
Output level selector	Controls the output voltage level according to the input control pin (M and DISPOFFB) (refer to Section 4-2).	COM / SEG
20x4-bit segment data BI-directional shift register	Stores output data value by shifting the input values. In 1-bit serial interface mode application, all 80 shift clocks (SCK) are needed to store all the display data. But in 4-bit parallel transfer mode application, only 20 clocks are needed. In common driver application mode, this block does not work.	SEG
80-bit data latch / common data BI-directional shift register	In segment driver application mode, the data from the 20x4-bit segment data shift register are latched for segment driver output. In single-type common driver application,1-bit input data (from DL or DR pin) is shifted and latched by the direction according to the SHL signal input. In dual-type common application mode, 80-bit registers are divided by two blocks and controlled independently (refer to Section 4-2-3).	COM / SEG
80-bit level shifter	Voltage level shifter block for high voltage part. The inputs of this block are of logical voltage level and the outputs of this block are at high voltage level value. These values are input in to the driver.	SEG
80-bit 4-level driver	Selects the output voltage level according to M and latched data value. If the data value is "High" the driver output is at selected voltage level (V0 or V5), and in the reverse case the driver output value is at the non-selected level (V12 or V43). In segment driver application mode, non-selected output value is V2 or V3. and when in common driver application, this value becomes V1 or V4.	SEG

4-2 Pin Description

<table>
<tr><th>Pin</th><th>I/O</th><th>Name</th><th>Description Function</th><th>Interface</th></tr>
<tr><td>VDD</td><td rowspan="3">P</td><td rowspan="3">Power supply</td><td>Logical "High" input port (+5V ± 10%, +3V ± 10%)</td><td rowspan="3">Power</td></tr>
<tr><td>VSS</td><td>0V (GND)</td></tr>
<tr><td>VEE</td><td>Logical "Low" for high voltage part</td></tr>
<tr><td>V0, V12, V43, V5</td><td>I</td><td>LCD driver output voltage level</td><td>Bias supply voltage input to drive the LCD. Bias voltage divided by the resistance is usually used as a supply voltage source (refer to Section 4-2-2).</td><td>Power</td></tr>
<tr><td>SC1 - SC80</td><td>O</td><td>LCD driver output</td><td>Display data output pin which corresponds to the respective latch contents. One of V0, V12, V34 and V5 is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to Section 4-2-1).</td><td>LCD</td></tr>
<tr><td>CL2</td><td>I</td><td>Data shift clock</td><td>Clock pulse input for the bi-directional shift register.
– In segment driver application mode, the data is shifted to 20 x 4-bit segment data shift.
The clock pulse, which was input when the enable bit (ELB/ERB) is in not active condition, is invalid.
– In common driver application mode, the data is shifted to 80-bit common data bi-directional shift register by the CL1 clock.Hence, this clock pin is not used (Open or connect this pin to VDD).</td><td>Controller</td></tr>
<tr><td>M</td><td>I</td><td>AC signal for LCD driver output</td><td>Alternate signal input pin for LCD driving.
Normal frame inversion signal is input in to this pin.</td><td>Controller</td></tr>
<tr><td>CL1</td><td>I</td><td>Data latch clock</td><td>– In segment driver application mode, this signal is used for latching the shift register contents at the falling edge of this clock pulse. CL1 pulse "High" level initializes power-down function block.
– In common driver application mode, CL1 is used as a shifting clock of common output data.</td><td>Controller</td></tr>
<tr><td>DISPOFFB</td><td>I</td><td>Display OFF control</td><td>Control input pin to fix the driver output (SC1~SC80) to V0 level,during "Low" value input. LCD becomes non-selected by V0 level output from every output of segment drivers and every output of common drivers.</td><td>Controller</td></tr>
<tr><td>CS</td><td>I</td><td>COM / SEG mode control</td><td>When CS = "Low", RA0086A is used as an 80-bit segment driver.
When CS = "High", RA0086A is set to an 80-bit common driver</td><td>VDD/ VSS</td></tr>
<tr><td>AMS</td><td>I</td><td>Application mode select</td><td>According to the input value of the AMS and the CS pin, application mode of RA0086AA is differs as shown below.
<table>
<tr><th>CS</th><th>AMS</th><th>Application mode</th><th>COM /SEG</th></tr>
<tr><td>0</td><td>0</td><td>4-bit parallel interface mode.</td><td rowspan="2">SEG</td></tr>
<tr><td>0</td><td>1</td><td>1-bit serial interface mode.</td></tr>
<tr><td>1</td><td>0</td><td>Single type application mode</td><td rowspan="2">COM</td></tr>
<tr><td>1</td><td>1</td><td>Dual type application mode</td></tr>
</table></td><td>VDD/ VSS</td></tr>
</table>

<table>
<tr><td>D1_SID, D2_DL, D3_DM, D4_DR.</td><td>I/O</td><td>Display data input / Serial input data / left,right data input output</td><td>- In segment driver application mode, these pins are used as 4-bit data input pin (when 4-bit parallel interface mode : AMS = "Low"), or D1_SID is used as serial data input pin and other pins are not used (connect these to VDD) (when 1-bit serial interface mode : AMS = "High").

– In common driver application mode, the data is shifted from D2_DL(D4_DR) to D4_DR(D2_DL), when in single type interface mode (AMS = "Low"). In dual type application case, the data are shifted from D2_DL and D3_DM (D4_DR and D3_DM) to D4_DR(D2_DL). In each case the direction of the data shift and the connection of data pins are determined by SHL input (refer to Section 4-2-3、4-2-4).</td><td>Controller</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction control</td><td>When SHL = "Low", data is shifted from left to right.
When SHL = "High", the direction is reversed. (refer to Section 4-2-3)</td><td>VDD/ VSS</td></tr>
<tr><td>ELB,ERB</td><td>I/O</td><td>Enable data input/output</td><td>– In segment driver application mode, the internal operation is enabled only when enable input (ELB or ERB) is “Low” (power down function). When several drivers are serially connected, the enable state of each driver is shifted according to the SHL input. Connect these pins as below.
<table>
<tr><td rowspan="2">SHL</td><td colspan="2">Segment Driver</td></tr>
<tr><td>ELB</td><td>ERB</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
</table>
- In common driver application mode, power down function is not used. Open these pins.</td><td></td></tr>
</table>

4-2-1 Output Voltage Level Control

Table 4-1

M	Latched Data	DISPOFFB	Output level (SC1 – SC80)	
			SEG Mode	COM Mode
L	L	H	V12 (V2)	V12 (V1)
L	H	H	V0	V5
H	L	H	V43 (V3)	V43 (V4)
H	H	H	V5	V0
X	X	L	V0	V0

4-2-2 LCD Driving Voltage Application Circuit

(1) Segment driver application (CS = "Low")

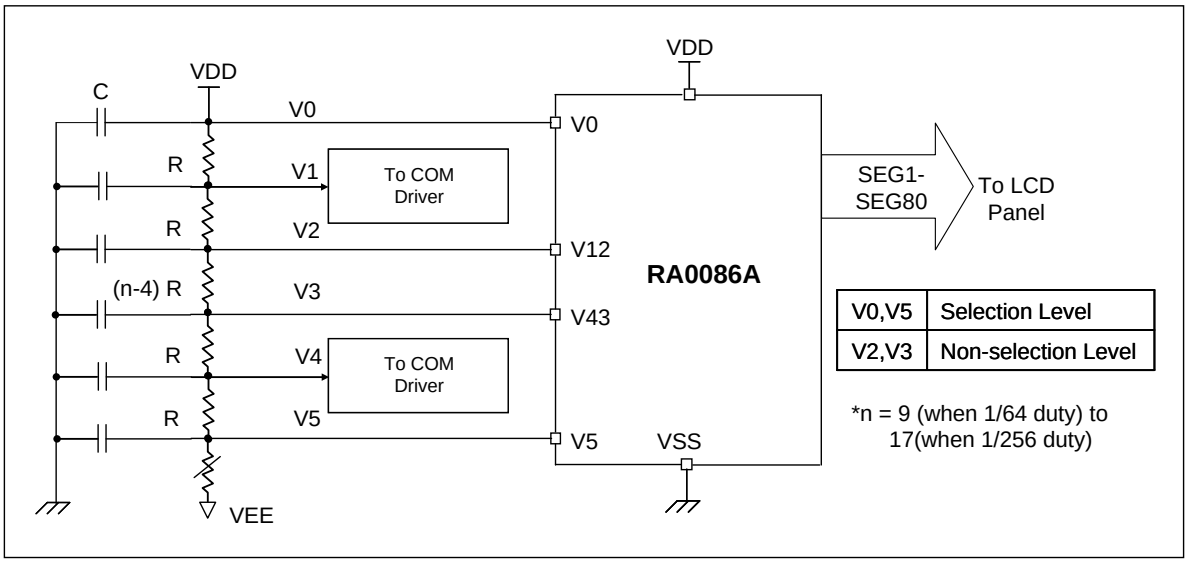


Figure 4-1

(2) Common driver application (CS = "High")

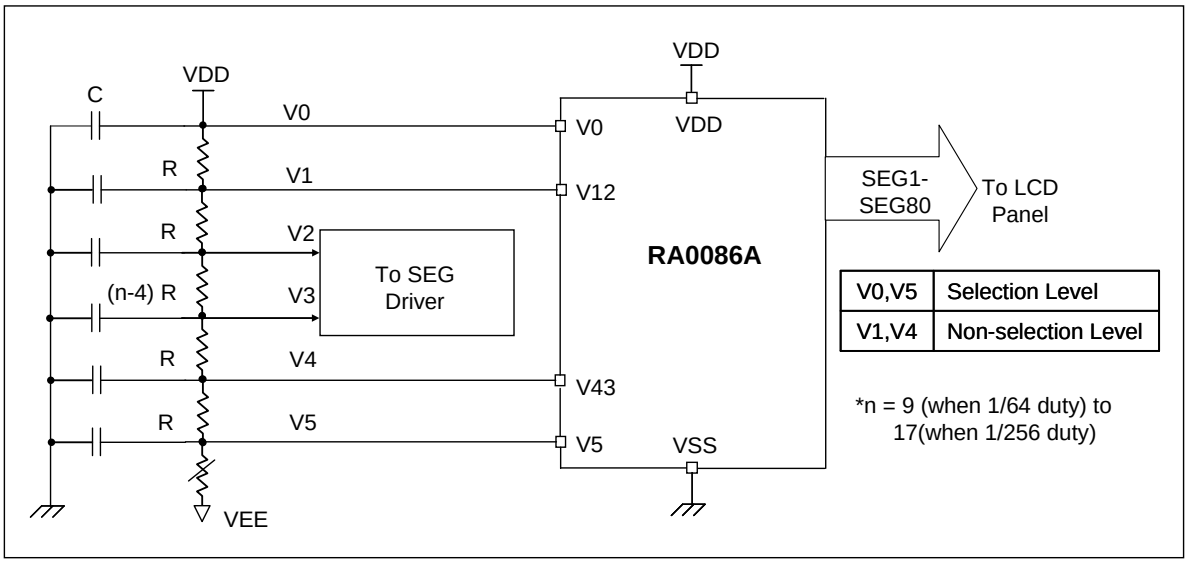
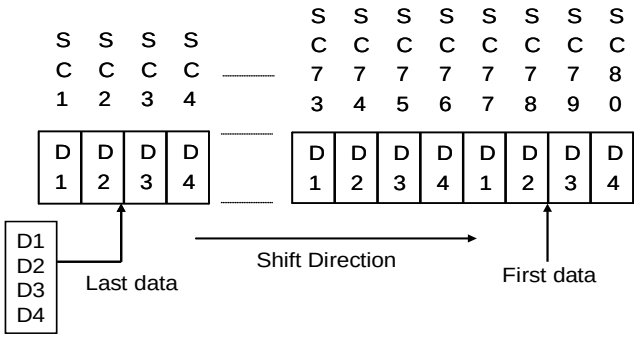
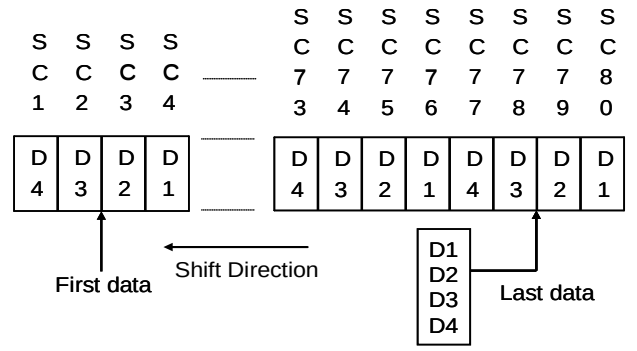
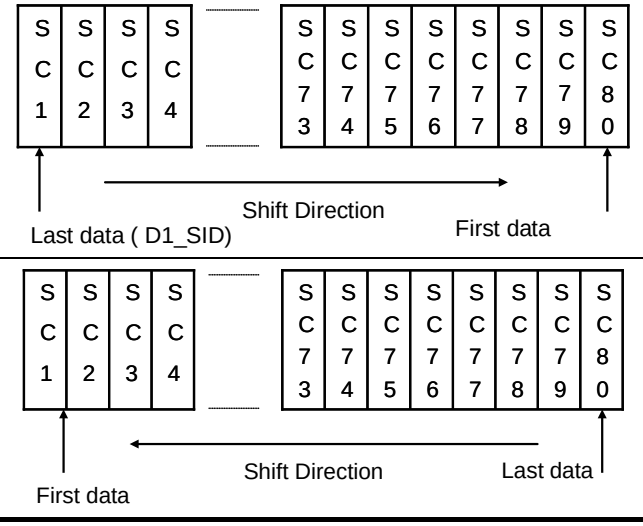


Figure 4-2

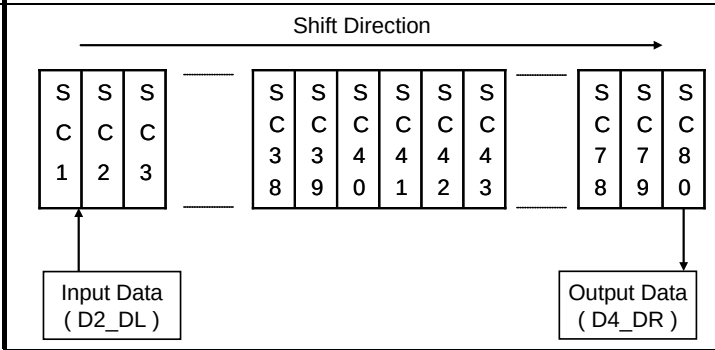
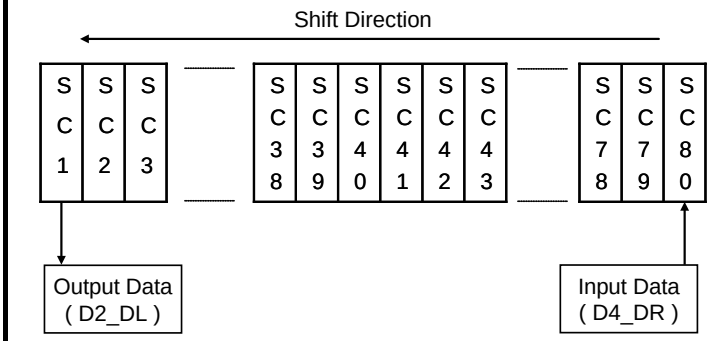
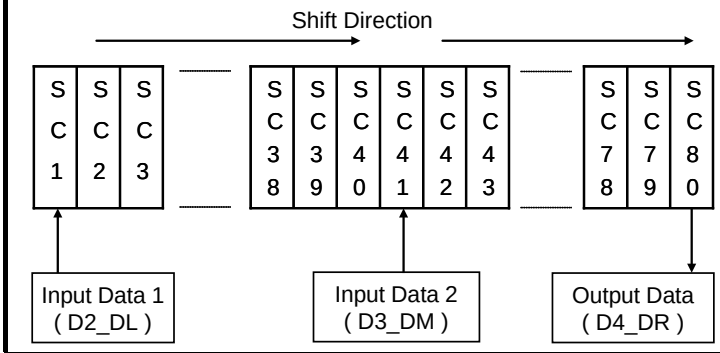
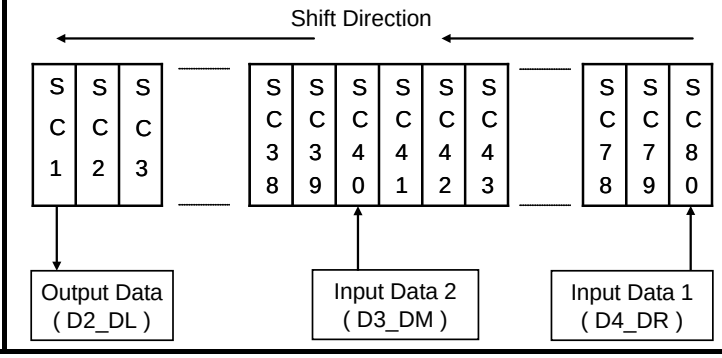
4-2-3 Data Shift Direction according to Control Signals

(1) When CS = "Low" (Segment driver application)

<table>
<tr><th>AMS</th><th>SHL</th><th>Application Mode</th><th>Data Direction</th><th>Input Pin</th></tr>
<tr><td rowspan="2">L</td><td>L</td><td rowspan="2">4-Bit Parallel Data Transfer Mode (SEG)</td><td rowspan="2"> 


</td><td rowspan="2">D1_SID, D2_DL, D3_DM, D4_DR</td></tr>
<tr><td>H</td></tr>
<tr><td rowspan="2">H</td><td>L</td><td rowspan="2">1-Bit Serial Data Transfer Mode (SEG)</td><td rowspan="2"> 
</td><td rowspan="2">D1_SID</td></tr>
<tr><td>H</td></tr>
</table>

(2) When CS = "High" (Common driver application)

AMS	SHL	Application Mode	Data Direction	Input Pin
L	L	Single-type Application Mode (COM)		D2_DL
	H			D4_DR
H	L	Dual-type Application Mode (COM)		D2_DL D3_DM
	H			D4_DR D3_DM

4-2-4 Usage of Data Pins

Table 4-2

COM /SEG (CS pin)	Application Mode (AMS pin)	SHL	Data Interface Pin			
			D1_SID	D2_DL	D3_DM	D4_DR
SEG (CS =Low)	4-bit parallel interface mode (AMS = Low)	X	D1 (input)	D2 (input2)	D3 (input3)	D4 (input4)
	1-bit serial interface mode (AMS = High)	X	SID (input)	Connect to VDD		
COM (CS =High)	single-type application mode (AMS = Low)	L	Open	DL (input)	Open	DR (output)
		H		DL (output)		DR (input)
	dual-type application mode (AMS =High)	L	Open	DL (input1)	DM (input2)	DR (output2)
		H		DL (output2)	DM (input2)	DR (input1)

5. Electrical Characteristics

5-1 Maximum Absolute Limit

Table 5-1

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{DD}	-0.3 - +7.0	V
Driver supply voltage	V_{LCD}	0 - +32	
Input voltage	V_{IN}	-0.3 - V_{DD}+0.3	
Operation temperature	T_{OPR}	-30 - +90	°C
Storage temperature	T_{STG}	-55 - +150	

NOTE : Voltage greater than above may damage to the circuit.

5-2 DC Characteristics

(1) Segment Driver Application

(V_{SS} = 0V, Ta = - 30 – +85°C)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
Operating voltage1	V_{DD}			2.7		5.5	V
	V_{LCD}	V_{IN} = V_{DD} - V_{EE}		6	-	30	
Input voltage (1)	V_{IH}	-		0.8V_{DD}	-	V_{DD}	
	V_{IL}	-		0	-	0.2V_{DD}	
Output voltage (2)	V_{OH}	I_{OH} = -0.4mA		V_{DD}-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	V_{IN} = V_{DD} to V_{SS}		-10	-	10	µA
Input leakage current 2 (3)	I_{IL2}	V_{IN} = V_{DD} to V_{EE}		-25	-	25	
On resistance(4)	R_{ON}	I_{ON} = 100µA		-	2	4	kΩ
Supply current (5)	I_{STBY}	f_{CL1} = 32kHz M = V_{SS}	V_{SS} pin	-	-	100	µA
	I_{DD}	f_{CL1} = 32kHz f_M = 80Hz	V_{DD} = 5V	-	-	5	mA
			V_{DD} = 3V	-	-	2	
	I_{EE}		V_{DD} = 5V	-	-	500	µA

NOTES:

(1) Applied to CL1, CL2, ELB, ERB, D1_SID - D4_DR, SHL, DISPOFFB, M, CS, AMS pin
(2) ELB, ERB pin
(3) V0, V12, V43, V5 pin
(4) VLCD = VDD - VEE, V0 = VDD = 5V, V5= VEE = -23 V
V12 = VDD-2/n(VLCD), V43 = VEE+2/n(VLCD), n = 17 (1/256 duty, 1/17 bias)
(5) V0 = VDD, V12 = 1.71V(VDD = 5V) or -0.06V (VDD = 3V),
V43 = -19.71 V(VDD = 5V) or -19.94V (VDD = 3V),
V5 = VEE = -23V, no-load condition (1/256 duty, 1/17 bias)
4-bit parallel interface mode
ISTBY :VDD = 5V, fCL2 = 5.12MHz, SHL = VSS,
DISPOFFB = VDD,
M = VSS, display data pattern = 0000
IDD : VDD = 3V, fCL2 = 4MHz, display data pattern = 0101
VDD = 5 V, fCL2 = 5.12MHz, display data pattern = 0101
IEE : VDD = 5V, fCL2 = 5.12MHz, display data pattern = 0101, VEE pin

(2) Common Driver Application

(V_{SS} = 0V, Ta = - 30 – +85°C)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
Operating voltage	V_{DD}			2.7	-	5.5	V
	V_{LCD}	V_{IN} = V_{DD} - V_{EE}		6	-	30	
Input voltage (1)	V_{IH}	-		0.8V_{DD}	-	V_{DD}	
	V_{IL}	-		0	-	0.2V_{DD}	
Output voltage (3)	V_{OH}	I_{OH} = -0.4mA		V_{DD}-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	V_{IN} = V_{DD} to V_{SS}		-10	-	10	µA
Input leakage current 2 (2)	I_{IL2}	V_{IN} = 0V, V_{DD} = 5V (PULL UP)		-50	-125	-250	
Input leakage current 3 (4)	I_{IL3}	V_{IN} = V_{DD} to V_{EE}		-25	-	25	
On resistance(5)	R_{ON}	I_{ON} = 100µA		-	2	4	kΩ
Supply current (6)	I_{STBY}	f_{CL1} = 32kHz M = V_{SS}	V_{SS} pin	-	-	100	µA
	I_{DD}	f_{CL1} = 32kHz f_M = 80Hz	V_{DD} = 5V	-	-	200	
			V_{DD} = 3V	-	-	120	
	I_{EE}		V_{DD} = 5V	-	-	150	

NOTES:

(1) Applied to CL1, D2_DL (SHL = LOW), D4_DR (SHL = HIGH), SHL, DISPOFFB, M, CS, AMS pin
(2) Pull-up input pins : CL2, D1_SID, D3_DM (AMS = HIGH), ELB (SHL = LOW), ERB (SHL = HIGH)
(3) D2_DL (SHL = HIGH) , D4_DR (SHL = LOW) pin
(4) V0, V12, V43, V5 pin
(5) VLCD = VDD-VEE, V0 = VDD = 5V, V5 = VEE = -23V
V12 = VDD-1/n(VLCD), V43 = VEE+1/n(VLCD), n = 17(1/256 duty, 1/17 bias)
(6) V0 = VDD, V12 = 3.35V (VDD = 5V) or 1.47V (VDD = 3V),
V43 = -21.35V (VDD = 5 V) or -21.47V (VDD = 3 V),
V5 = VEE = -23 V, no-load condition (1/256 duty, 1/17 bias)
single-type mode operation : AMS = VSS, SHL = VSS, DISPOFFB = VDD
D1_SID = D3_DM = VDD, D4_DR = OPEN, ELB = ERB = OPEN,
ISTBY : VDD = 5V, M = VSS, D2_DL = VSS
IDD : fM = 80Hz, D2_DL = VDD
VDD = 3 V, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
VDD = 5 V, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
IEE : fM = 80Hz, D2_DL = VDD
VDD = 5V, current through VEE Pin, display data pattern = 10000000..., 01000000..., 00100000..., 00010000...

5-3 AC Characteristics

(1) Segment Driver Application

(V_{SS} = 0V, Ta = - 30 – +85°C)

Characteristic	Symbol	Test Condition	(1) V_{DD} = 5V ±10%			(2) V_{DD} = 3V ±10%			Unit
			Min	Typ	Max	Min	Typ	Max	
Clock cycle time	t_{CY}	Duty = 50%	125	-	-	250	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise / fall time	t_R/t_F	-	-	-	-	-	-	30	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
Clock set-up time	t_{CS}	-	80	-	-	120	-	-	
Clock hold time	t_{CH}	-	80	-	-	120	-	-	
Propagation delay time	t_{PHL}	ELB Output	-	-	60	-	-	125	
		ERB Output			60			125	
ELB,ERB set-up time	t_{PSU}	ELB Input	30	-	-	65	-	-	
		ERB Input	30			65			
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	µs
DISPOFFB clear time	t_{CD}	-	100	-	-	100	-	-	ns
M – OUT propagation delay time	t_{PD1}	C_L = 15pF	-	-	1.0	-	-	1.2	µs
CL1 – OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB – OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	-	

(2)Common Driver Application

(V_{SS} = 0V, Ta = - 30 – +85°C)

Characteristic	Symbol	Test Condition	(1) V_{DD} = 5V ±10%			(2) V_{DD} = 3V ±10%			Unit
			Min	Typ	Max	Min	Typ	Max	
Clock cycle time	t_{CY}	Duty = 50%	250	-	-	500	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise / fall time	t_R/t_F	-	-	-	50	-	-	50	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	µs
DISPOFFB clear time	t_{CD}	-	100	-	-	100	-	-	ns
Output delay time	t_{DL}	C_L = 15pF			200			250	µs
M – OUT propagation delay time	t_{PD1}		-	-	1.0	-	-	1.2	
CL1 – OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB – OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	1.2	

(3) Segment Driver Application Timing

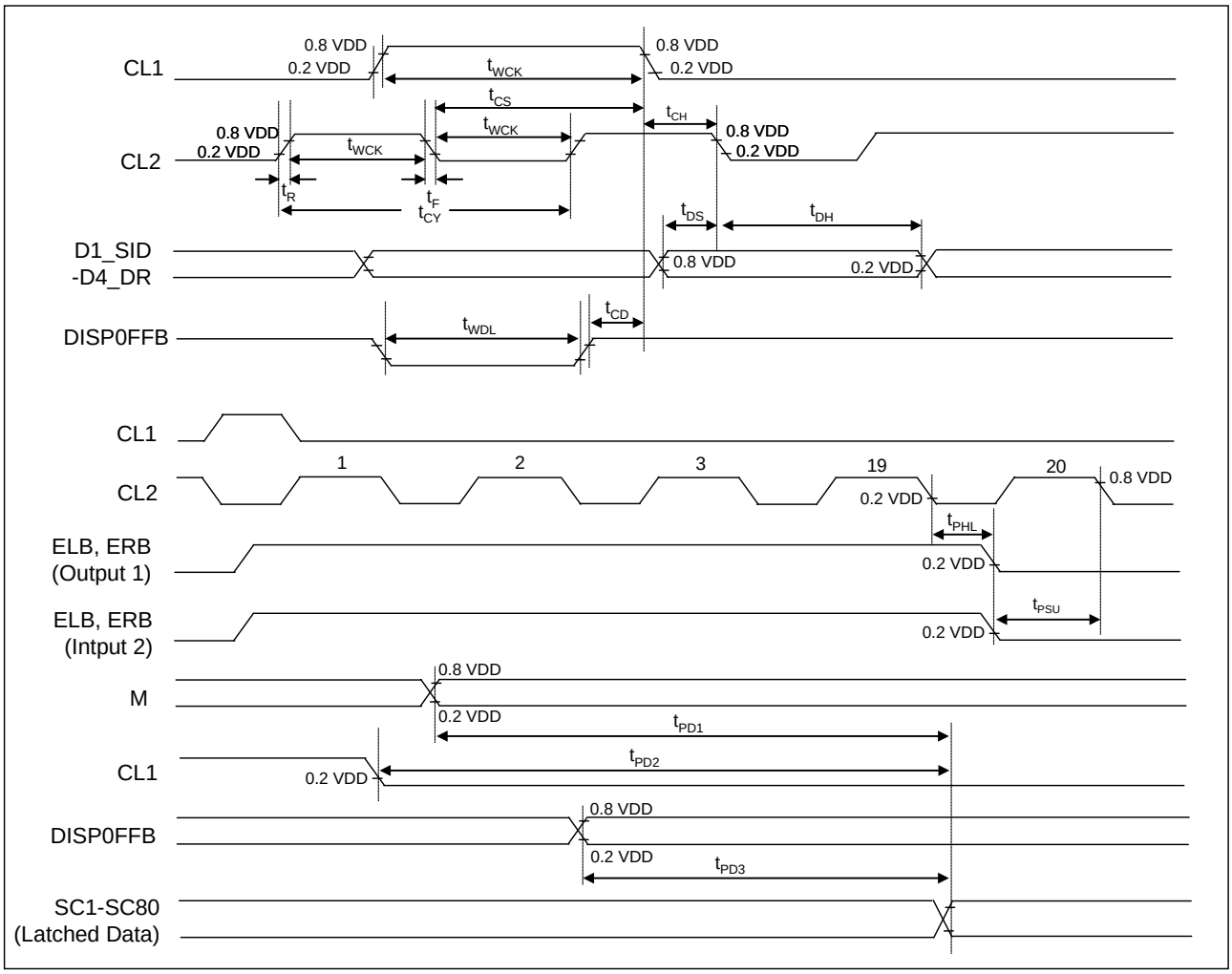
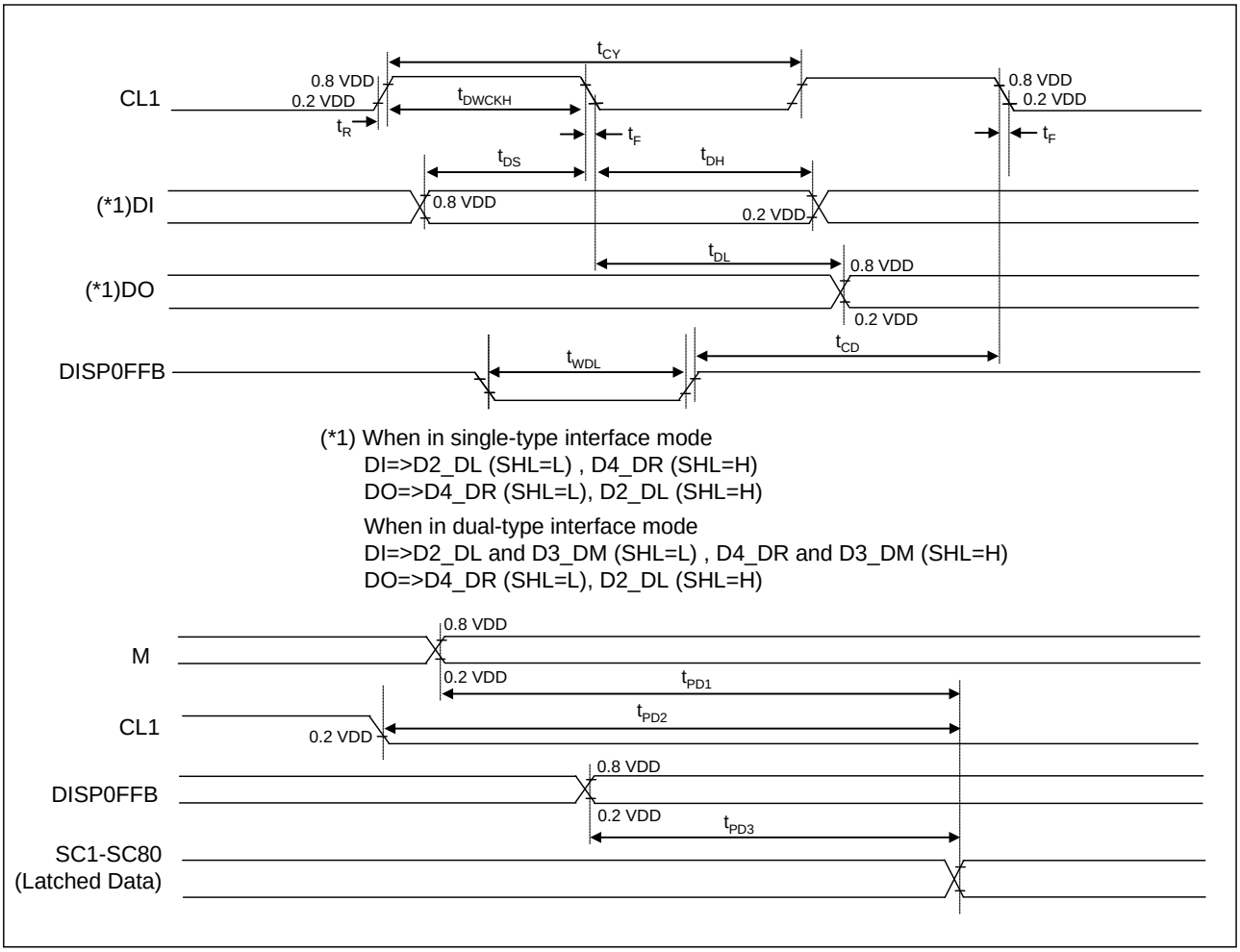


Figure 5-1

(4) Common Driver Application Timing



(*1) When in single-type interface mode
DI=>D2_DL (SHL=L) , D4_DR (SHL=H)
DO=>D4_DR (SHL=L), D2_DL (SHL=H)

When in dual-type interface mode
DI=>D2_DL and D3_DM (SHL=L) , D4_DR and D3_DM (SHL=H)
DO=>D4_DR (SHL=L), D2_DL (SHL=H)

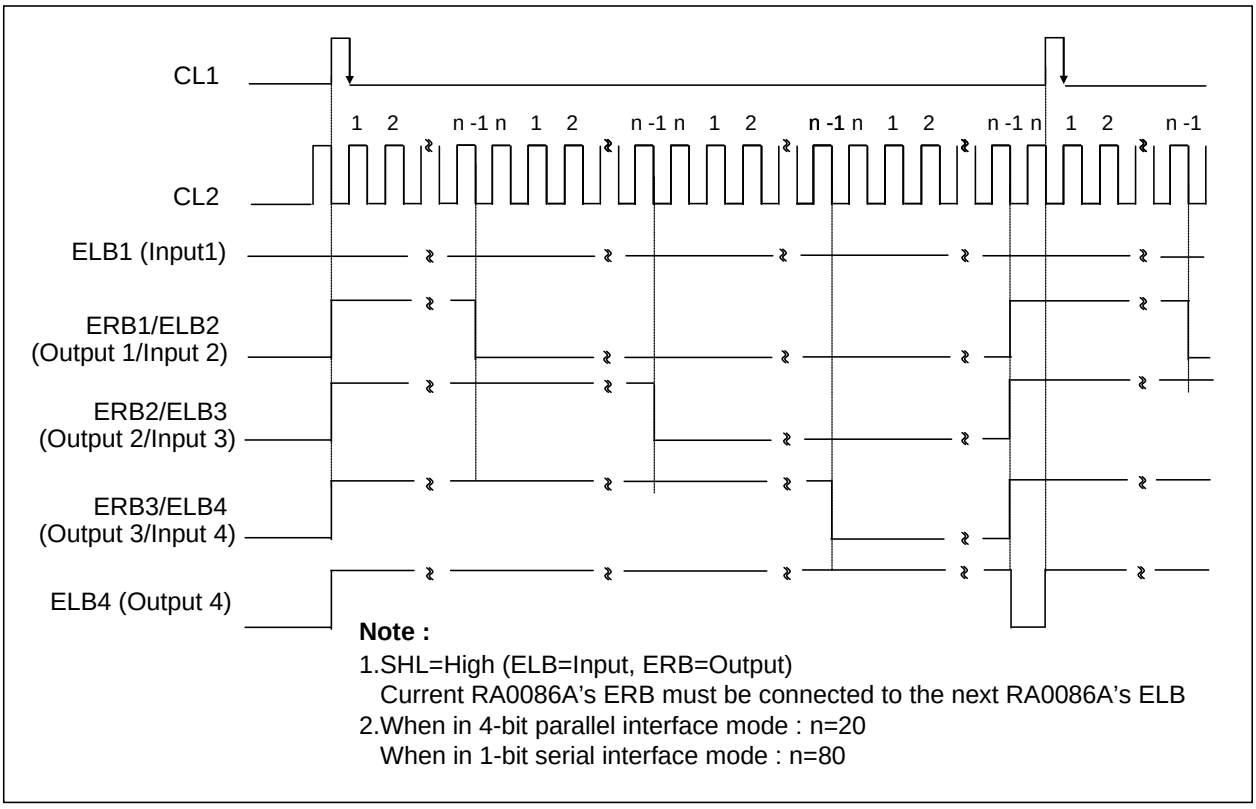
Figure 5-2

5-4 Power Down Function

In the case of cascade connection of segment mode drivers, RA0086A has a "power down function" in order to reduce the power consumption.

SHL	Enable Input	Enable Output	Current Driver Status	The Other Drivers Status
L	ERB	ELB	While ERB =Low, current driver is enabled.	Disabled
H	ELB	ERB	While ELB =Low, current driver is enabled.	Disabled

* In the case of common driver application, power down function does not work.



Note :

1.SHL=High (ELB=Input, ERB=Output)
Current RA0086A's ERB must be connected to the next RA0086A's ELB

2.When in 4-bit parallel interface mode : n=20
When in 1-bit serial interface mode : n=80

Figure 5-3

5-5 Operation Timing Diagram

5-5-1 4-bit Parallel Mode Interface Segment Driver

◆ When SHL = Low

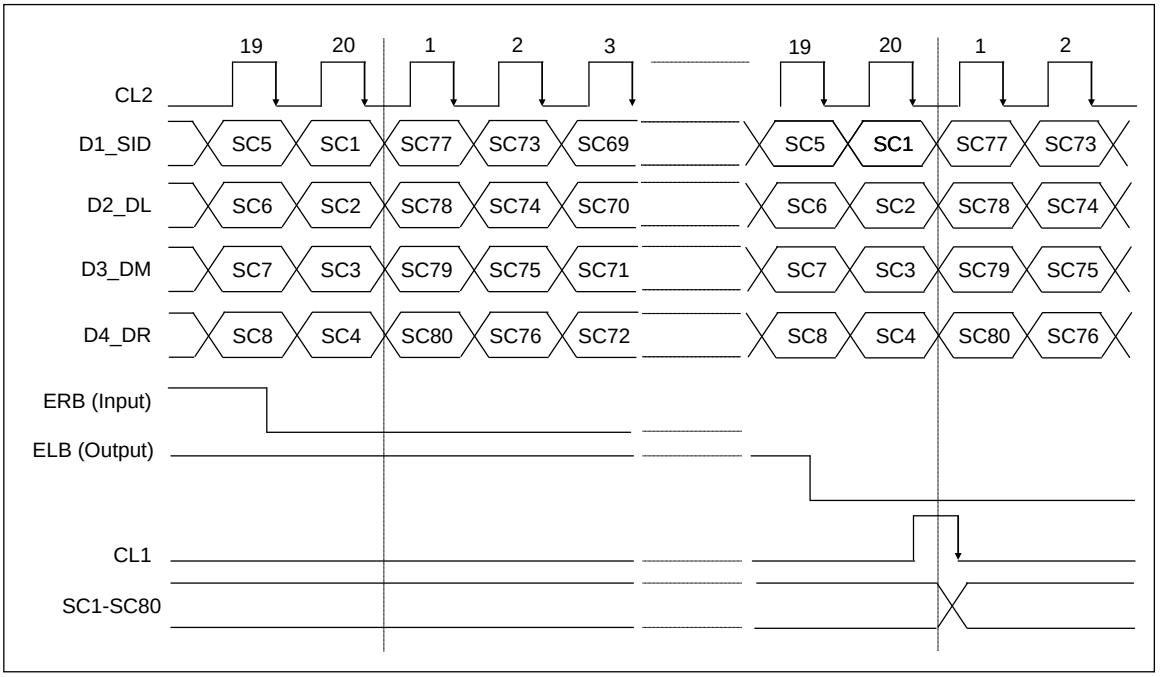


Figure 5-4

◆ When SHL = High

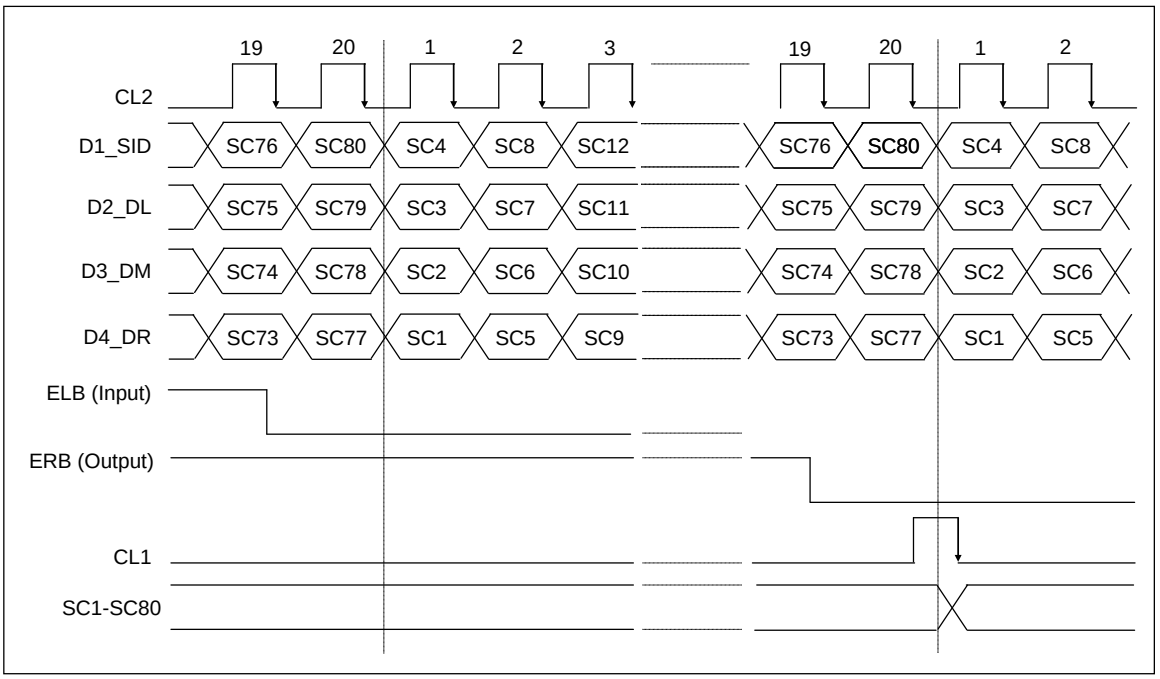


Figure 5-5

5-5-2 1-bit Serial Mode Interface Segment Driver

◆ When SHL = Low

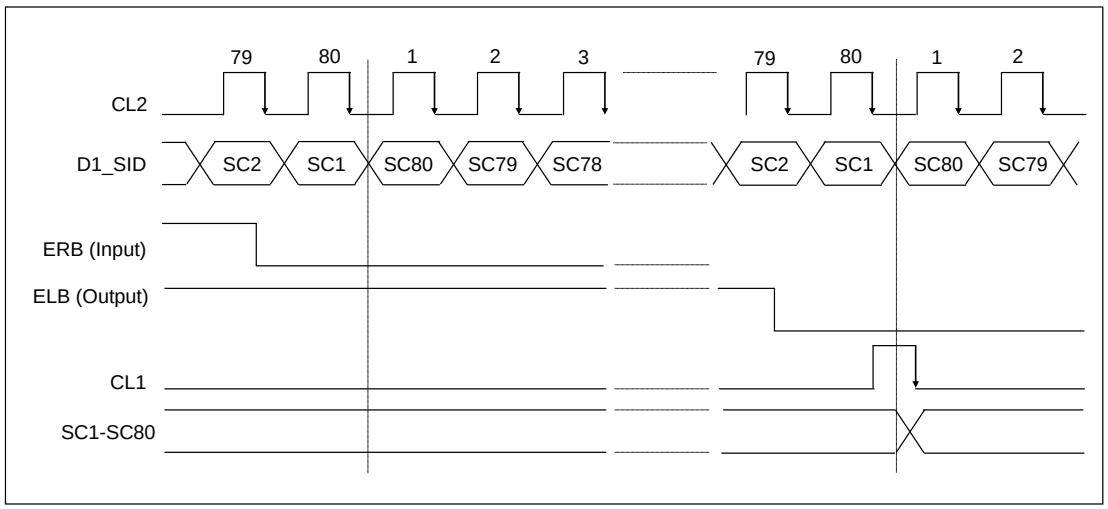


Figure 5-6

◆ When SHL = High

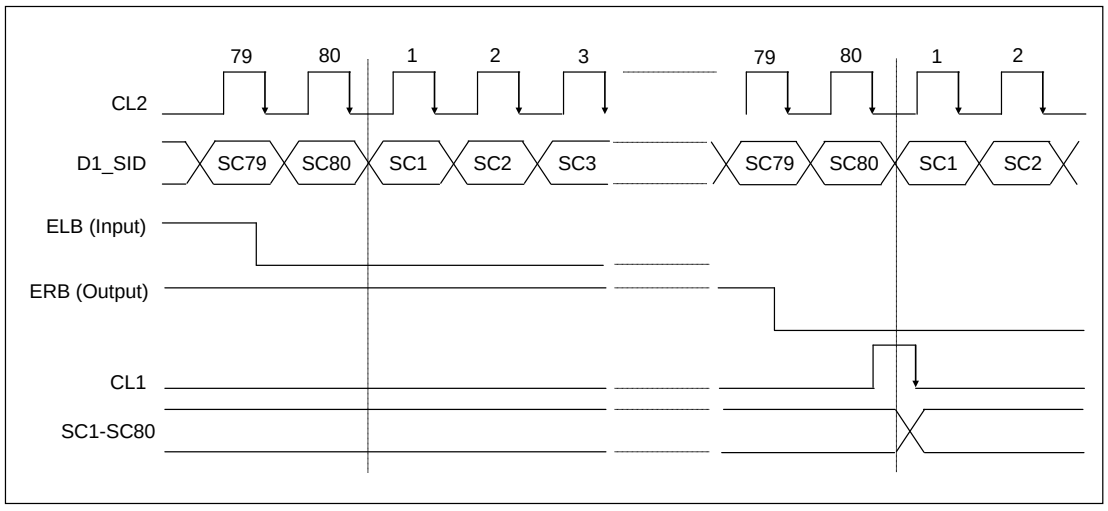


Figure 5-7

5-5-3 Single-type Interface Mode Common Driver

◆ When SHL = Low

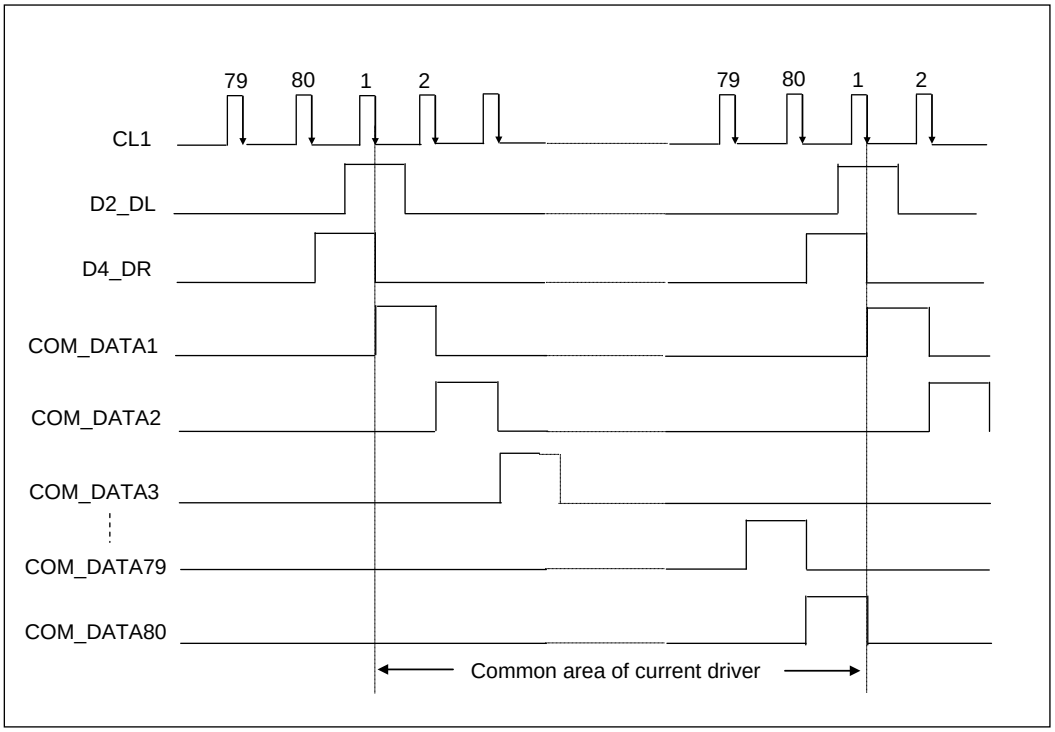


Figure 5-8

◆ When SHL = High

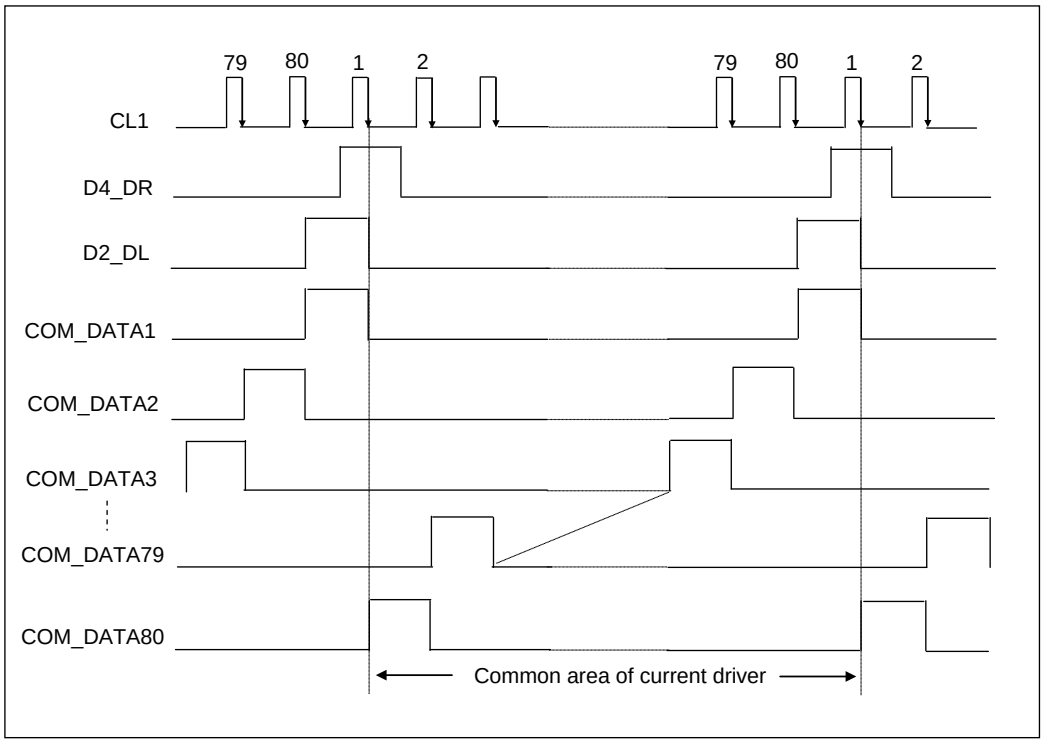


Figure 5-9

5-5-4 Dual-type Interface Mode Common Driver

◆ When SHL = Low

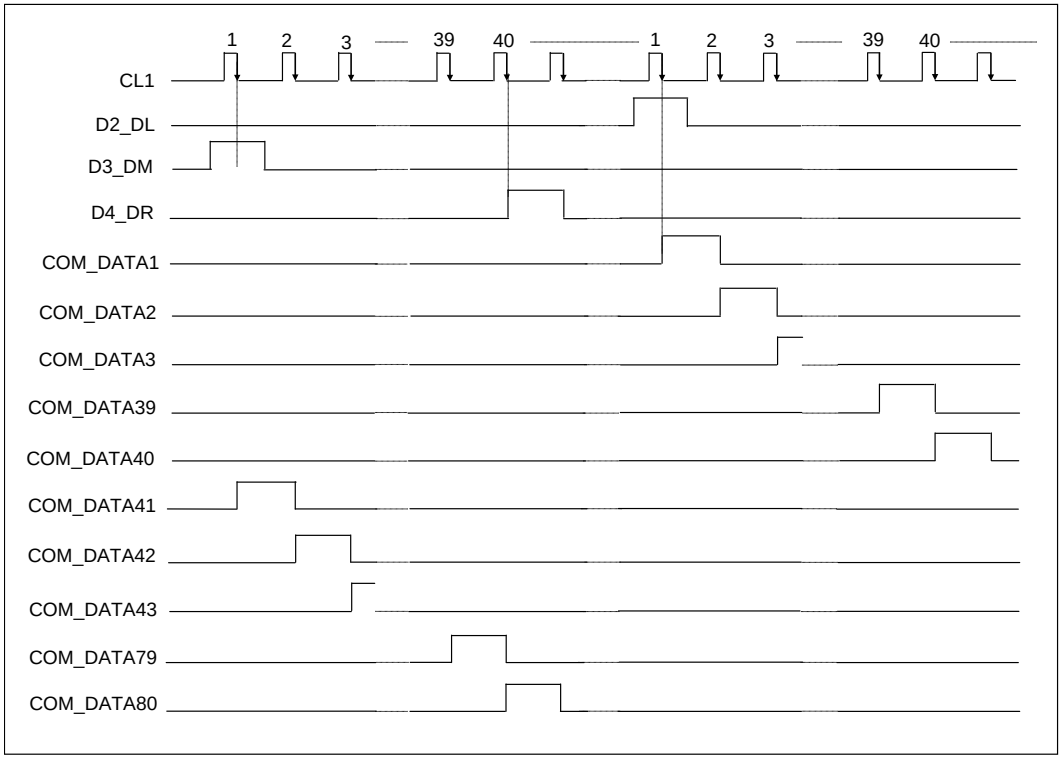


Figure 5-10

◆ When SHL = High

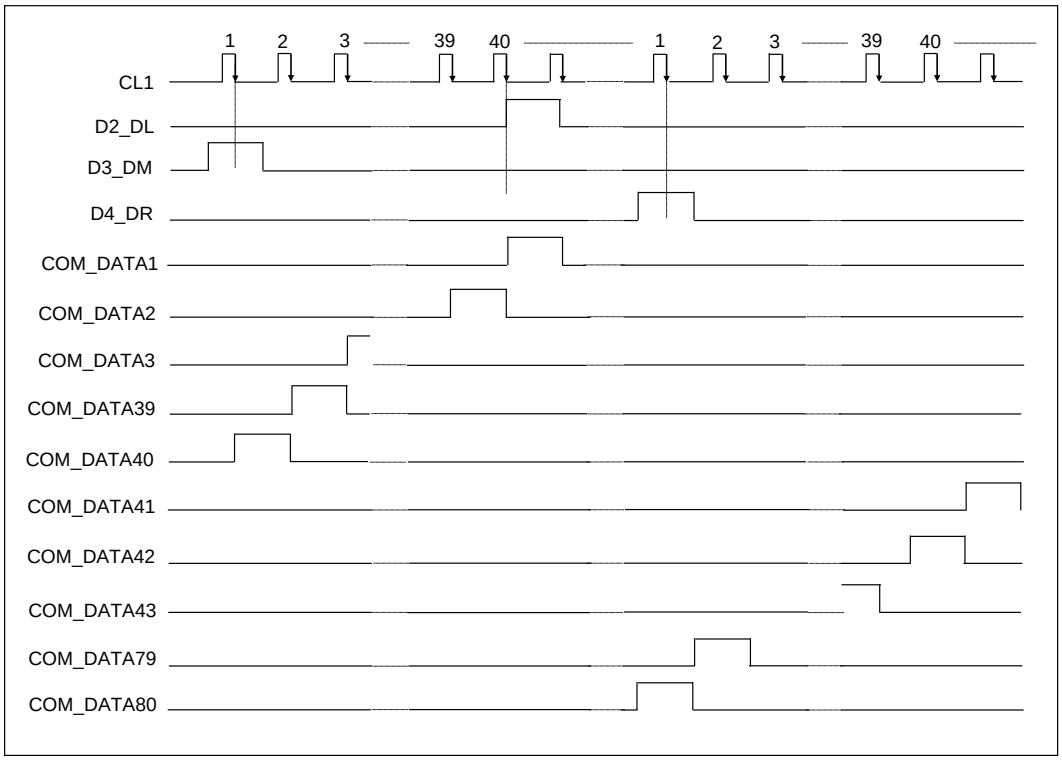


Figure 5-11

5-5-5 Common / Segment Driver Timming (1/200 Duty)

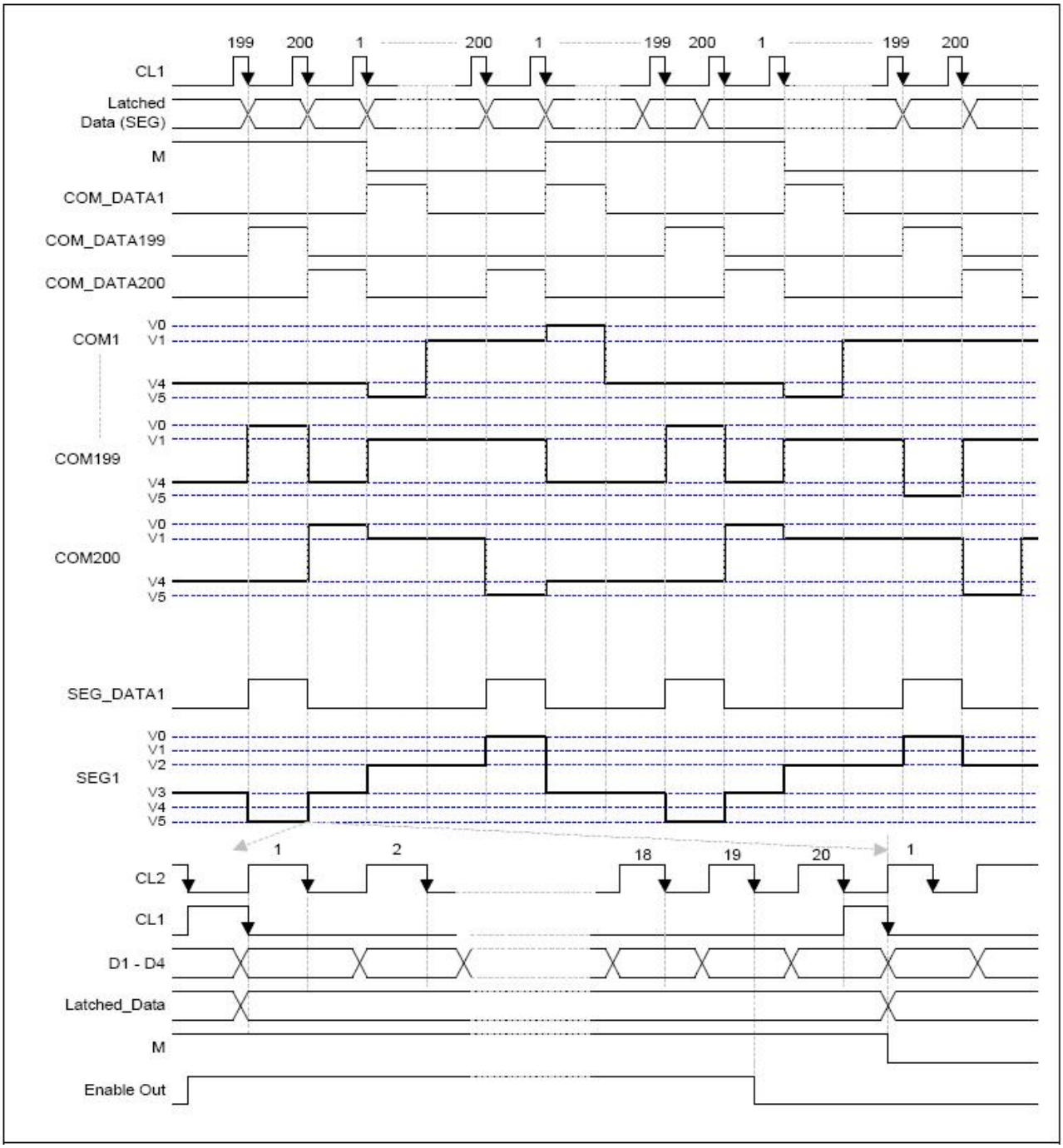


Figure 5-12

6. Application Information

6-1 4-bit Parallel Interface Mode (80-Ch. Segment Driver)

(1) Lower View (SHL = L, AMS = L)

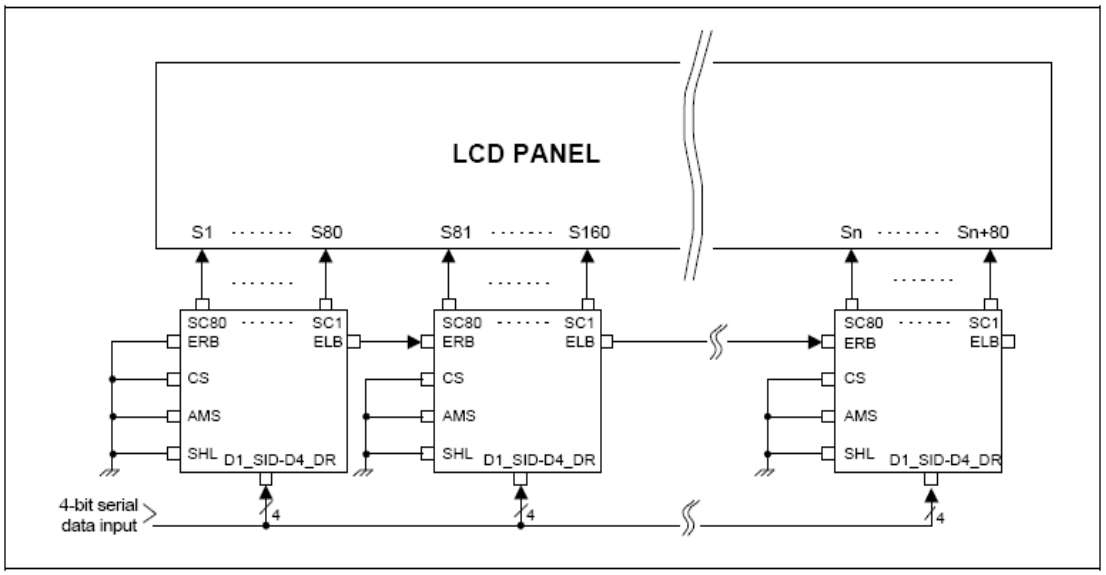


Figure 6-1

(2) Upper View (SHL = H, AMS = L)

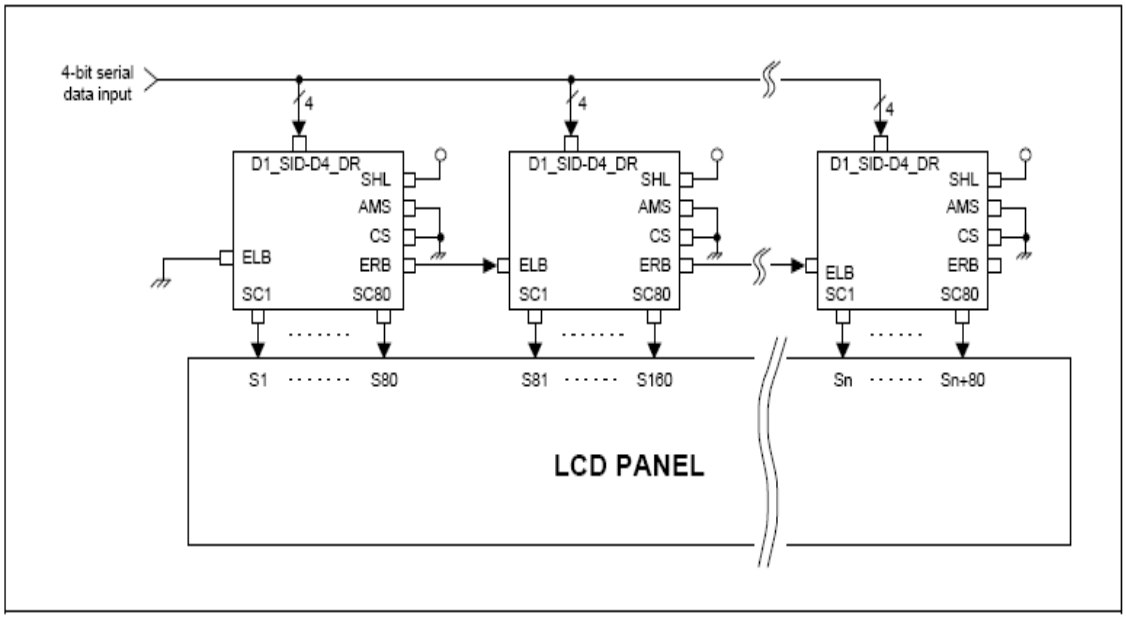


Figure 6-2

6-2 1-bit Serial Interface Mode (80-Ch. Segment Driver)

(1) Lower View (SHL = L, AMS = H)

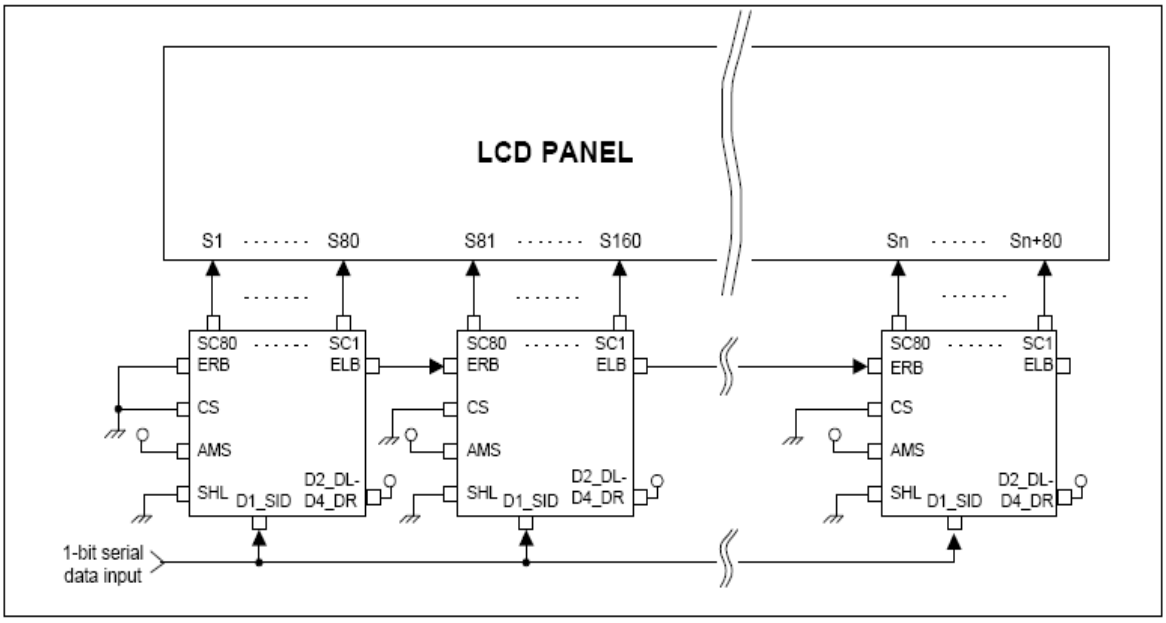


Figure 6-3

(2) Upper View (SHL = H, AMS = H)

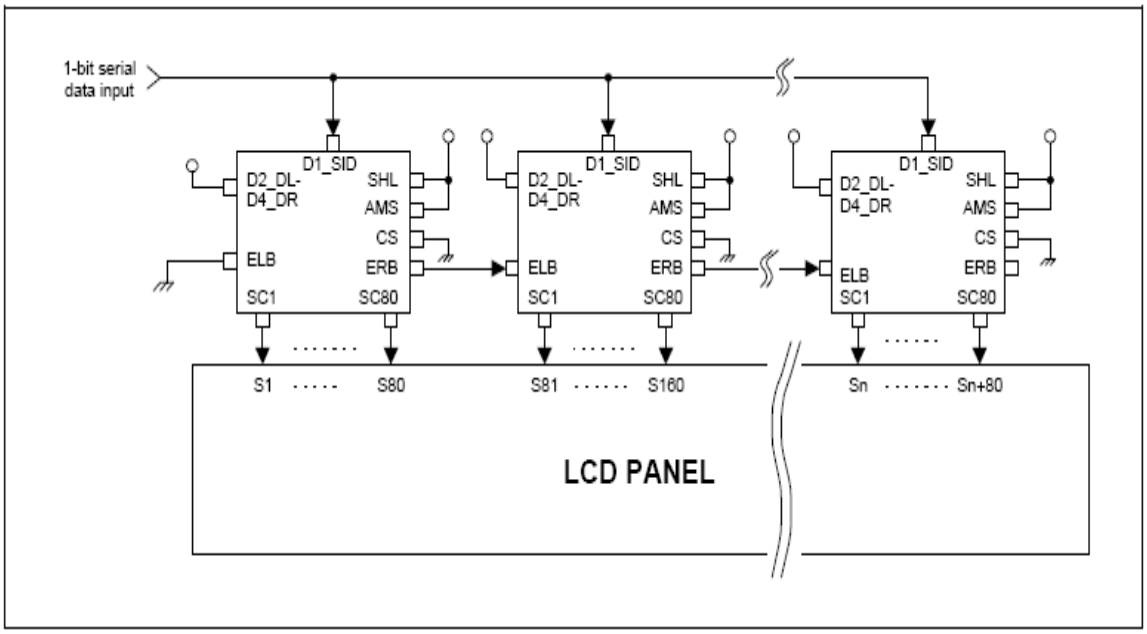


Figure 6-4

6-3 Single-type Interface Mode (80-Ch. Common Driver)

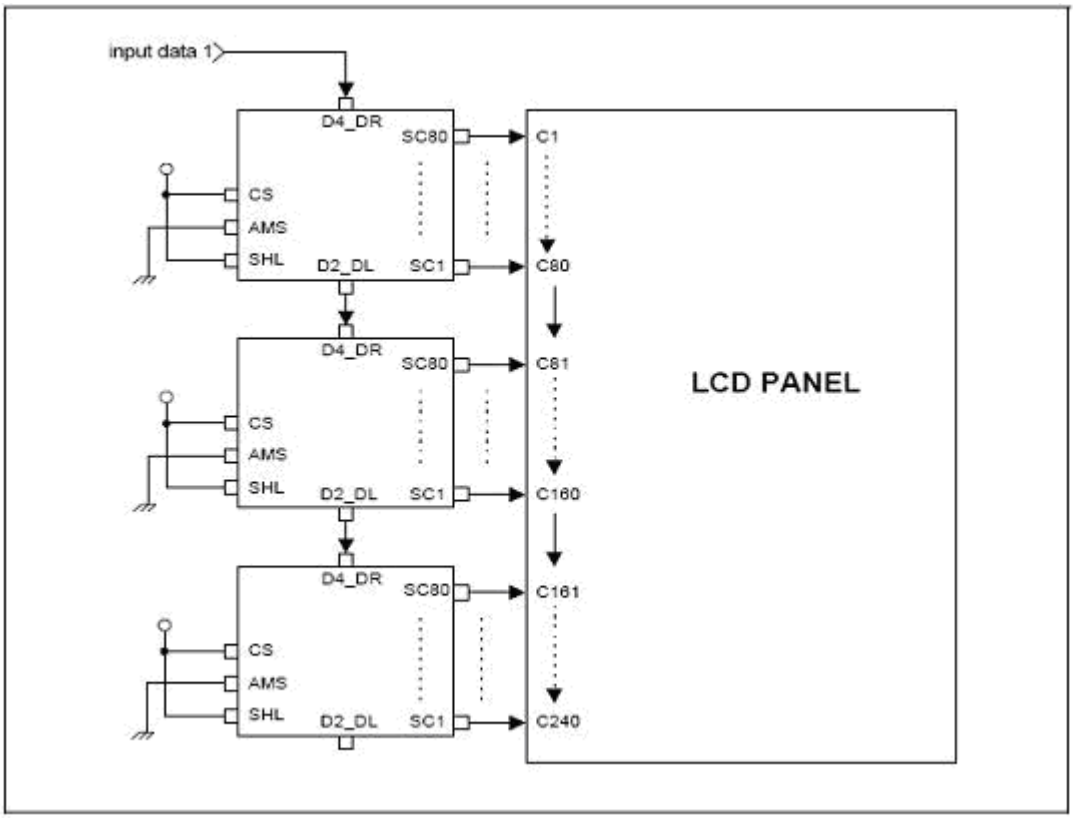


Figure 6-5

6-4 Dual-type Interface Mode (40-Ch. + 40-Ch. Common Driver)

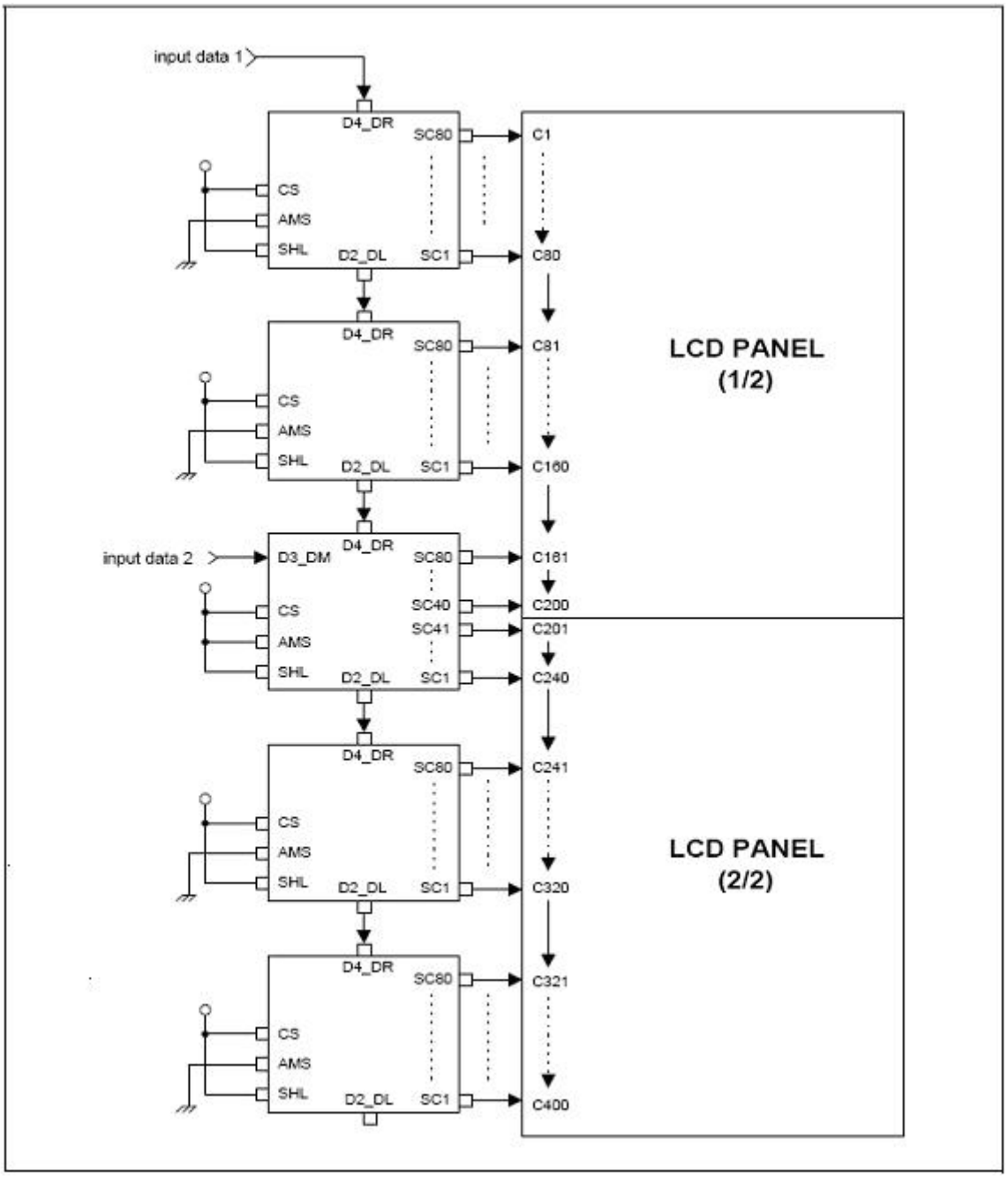


Figure 6-6

NOTE: Using this application mode (dual-type common mode), the duty ratio can be reduced to half. In case, 1/200 duty can be used to drive the 400 common LCD panel.

6-5 Application Circuit Example

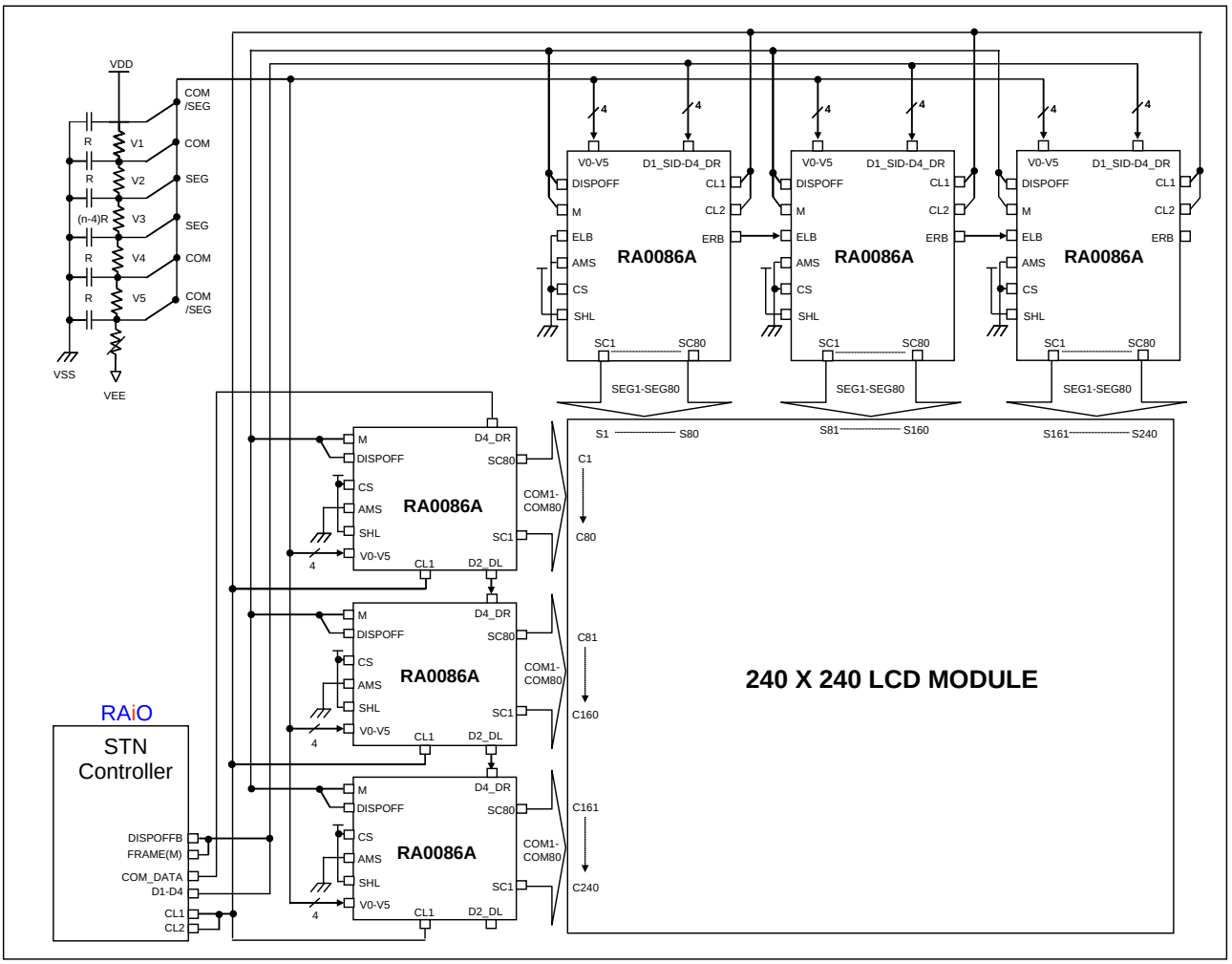


Figure 6-7 : Application Circuit

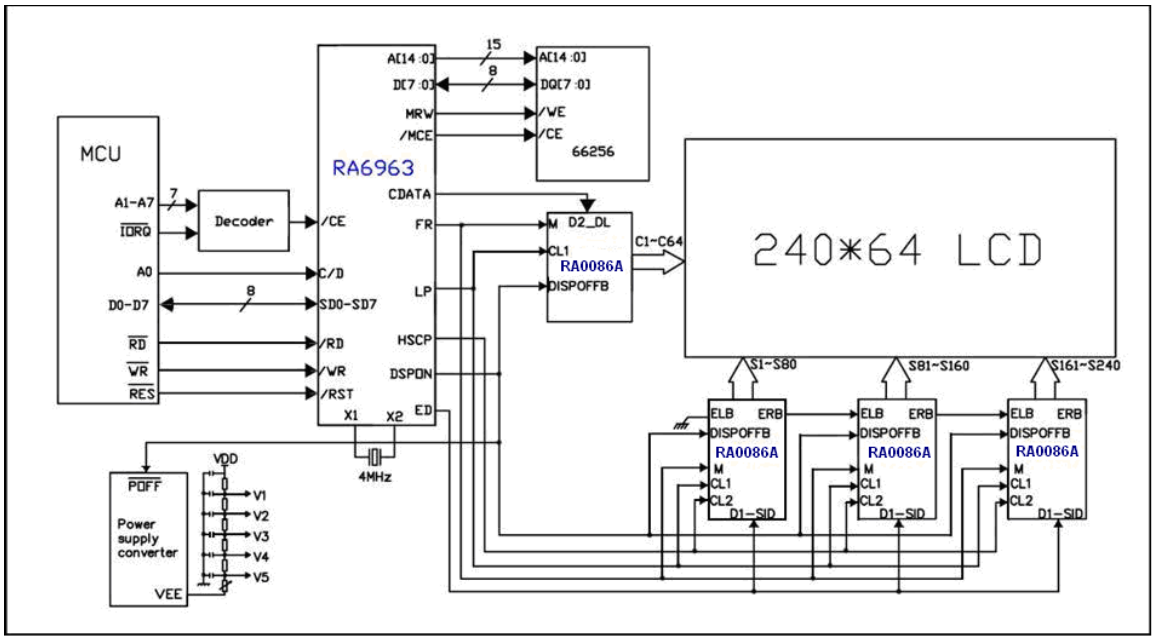


Figure 6-8 : RA6963 with RA0086A Application Circuit

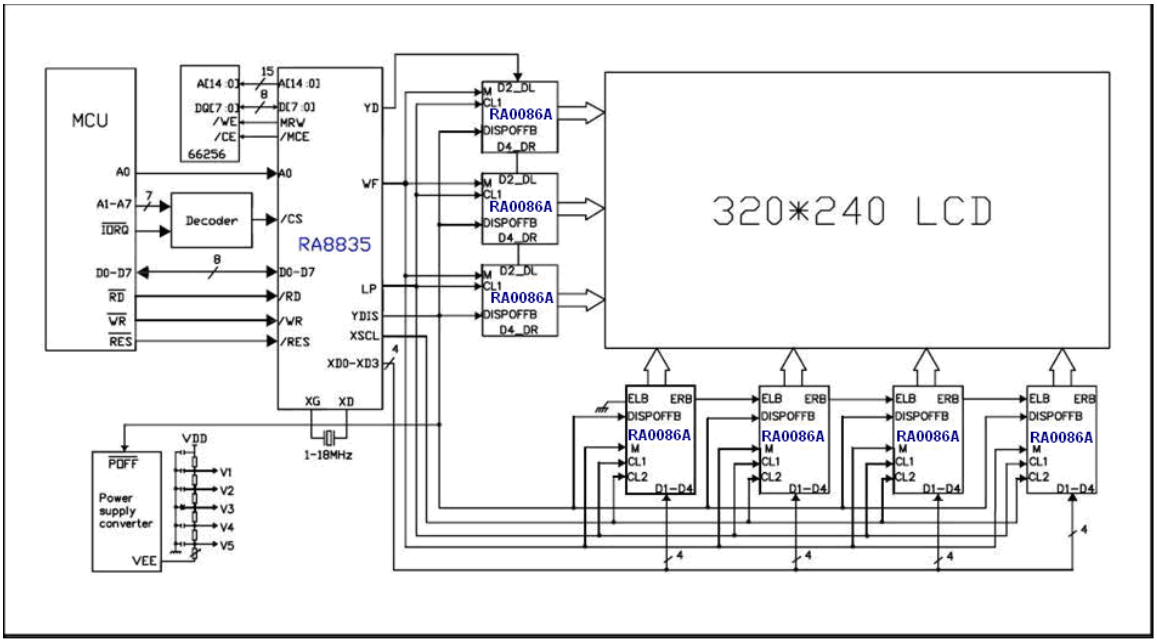


Figure 6-9 : RA8835 with RA0086A Application Circuit

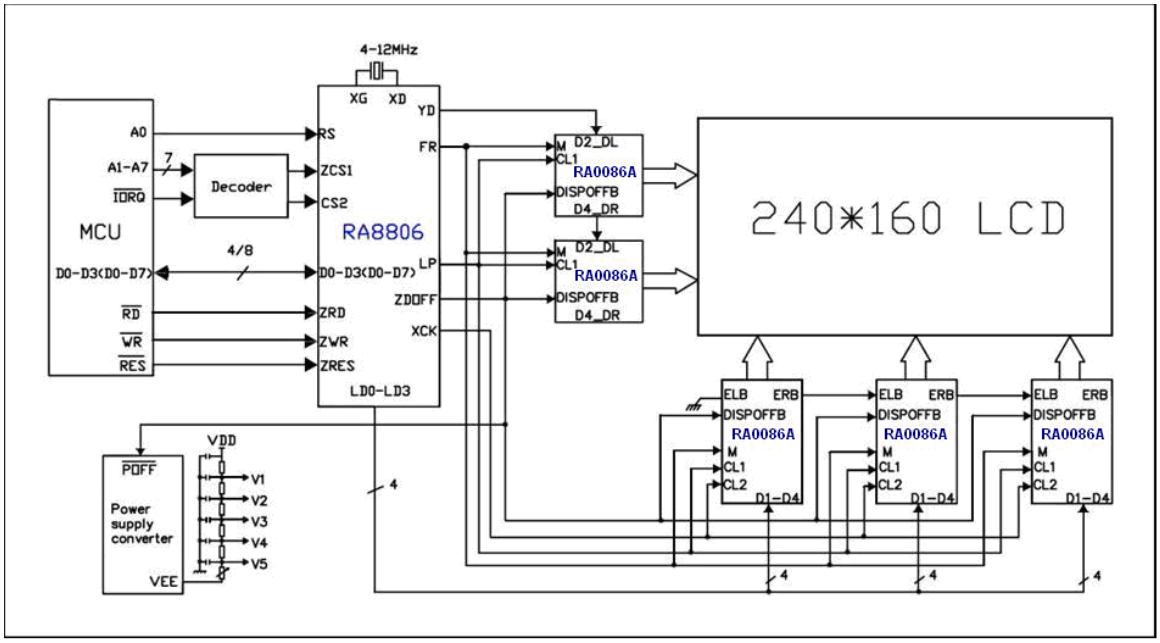
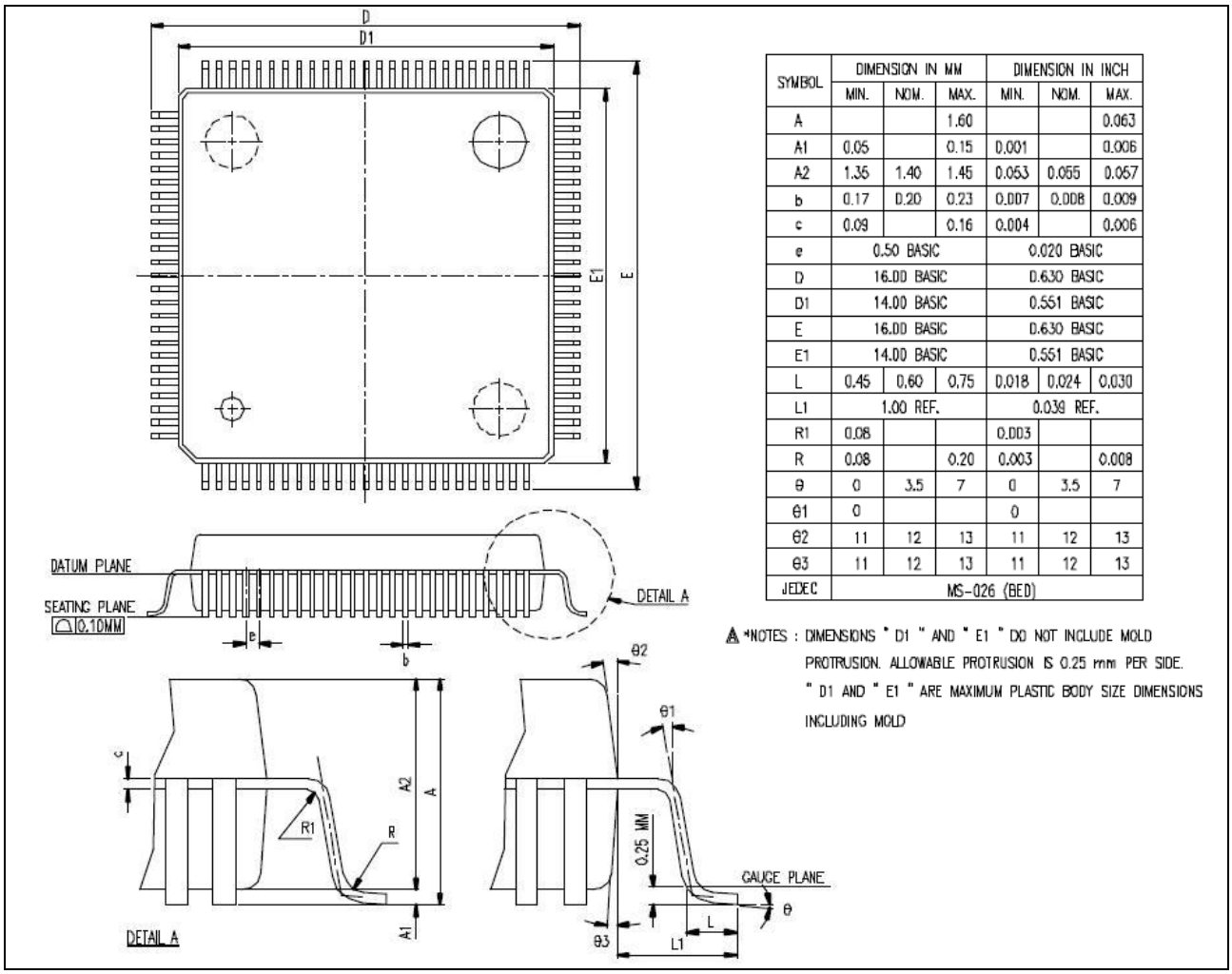


Figure 6-10 : RA8806 with RA0086A Application Circuit

7. Package

7-1 Package Information



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.001		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09		0.16	0.004		0.006
e	0.50 BASIC			0.020 BASIC		
D	16.00 BASIC			0.630 BASIC		
D1	14.00 BASIC			0.551 BASIC		
E	16.00 BASIC			0.630 BASIC		
E1	14.00 BASIC			0.551 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R	0.08		0.20	0.003		0.008
θ	0	3.5	7	0	3.5	7
θ1	0			0		
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
JEDEC	MS-026 (BED)					

⚠ *NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. " D1 AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD

Figure 7-1

7-2 Die Form

NOTE : Please connect the substrate to VDD or floating.

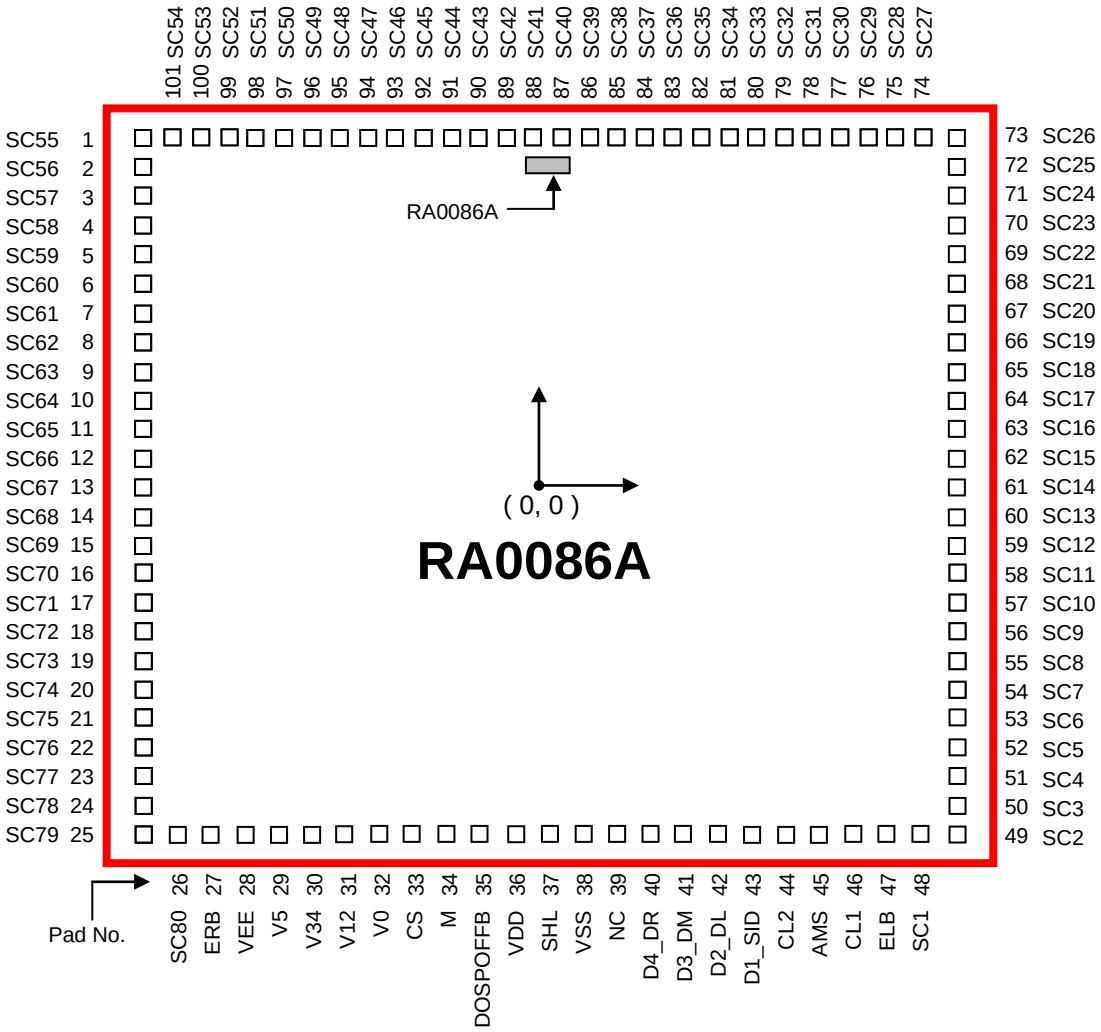


Figure 7-2

NOTE：Die Size=3168*2535um

Table 7-1

Die Size	3168*2535um
Pad Size 1	Pad #27~#47 : 80*65um
Pad Size 2	Pad #1~#26, #48~#101 : 68*65um

Table 7-2

Parts Number	Package
RA0086A	Die
RA0086AL3N	LQFP-100 pin

7-3 PAD Coordinate

Pad No.	Pad Name	X-axis	Y-axis
1	SC55	-1478.9	1120.3
2	SC56	-1478.9	1029.3
3	SC57	-1478.9	938.3
4	SC58	-1478.9	847.3
5	SC59	-1478.9	756.3
6	SC60	-1478.9	665.3
7	SC61	-1478.9	574.3
8	SC62	-1478.9	483.3
9	SC63	-1478.9	392.3
10	SC64	-1478.9	301.3
11	SC65	-1478.9	210.3
12	SC66	-1478.9	119.3
13	SC67	-1478.9	28.3
14	SC68	-1478.9	-62.7
15	SC69	-1478.9	-153.7
16	SC70	-1478.9	-244.7
17	SC71	-1478.9	-335.7
18	SC72	-1478.9	-426.7
19	SC73	-1478.9	-517.7
20	SC74	-1478.9	-608.7
21	SC75	-1478.9	-699.7
22	SC76	-1478.9	-790.7
23	SC77	-1478.9	-881.7
24	SC78	-1478.9	-972.7
25	SC79	-1478.9	-1063.7
26	SC80	-1312.4	-1114.1
27	ERB	-1171.4	-1112.9
28	VEE	-1049.5	-1112.9
29	V5	-934.5	-1112.9
30	V34	-819.5	-1112.9
31	V12	-696.2	-1112.9
32	V0	-581.2	-1112.9
33	CS	-466.2	-1112.9
34	M	-351.2	-1112.9
35	DISPOFFB	-236.2	-1112.9

Pad No.	Pad Name	X-axis	Y-axis
36	VDD	-121.2	-1112.9
37	SHL	-6.2	-1112.9
38	VSS	108.8	-1112.9
39	NC	237.6	-1112.9
40	D4_DR	366.4	-1112.9
41	D3_DM	481.4	-1112.9
42	D2_DL	596.4	-1112.9
43	D1_SID	711.4	-1112.9
44	CL2	826.4	-1112.9
45	AMS	941.4	-1112.9
46	CL1	1056.4	-1112.9
47	ELB	1171.4	-1112.9
48	SC1	1312.4	-1114.1
49	SC2	1478.9	-1063.7
50	SC3	1478.9	-972.7
51	SC4	1478.9	-881.7
52	SC5	1478.9	-790.7
53	SC6	1478.9	-699.7
54	SC7	1478.9	-608.7
55	SC8	1478.9	-517.7
56	SC9	1478.9	-426.7
57	SC10	1478.9	-335.7
58	SC11	1478.9	-244.7
59	SC12	1478.9	-153.7
60	SC13	1478.9	-62.7
61	SC14	1478.9	28.3
62	SC15	1478.9	119.3
63	SC16	1478.9	210.3
64	SC17	1478.9	301.3
65	SC18	1478.9	392.3
66	SC19	1478.9	483.3
67	SC20	1478.9	574.3
68	SC21	1478.9	665.3
69	SC22	1478.9	756.3
70	SC23	1478.9	847.3

Pad No.	Pad Name	X-axis	Y-axis
71	SC24	1478.9	938.3
72	SC25	1478.9	1029.3
73	SC26	1478.9	1120.3
74	SC27	1228.5	1162.1
75	SC28	1137.5	1162.1
76	SC29	1046.5	1162.1
77	SC30	955.5	1162.1
78	SC31	864.5	1162.1
79	SC32	773.5	1162.1
80	SC33	682.5	1162.1
81	SC34	591.5	1162.1
82	SC35	500.5	1162.1
83	SC36	409.5	1162.1
84	SC37	318.5	1162.1
85	SC38	227.5	1162.1
86	SC39	136.5	1162.1
87	SC40	45.5	1162.1
88	SC41	-45.5	1162.1
89	SC42	-136.5	1162.1
90	SC43	-227.5	1162.1
91	SC44	-318.5	1162.1
92	SC45	-409.5	1162.1
93	SC46	-500.5	1162.1
94	SC47	-591.5	1162.1
95	SC48	-682.5	1162.1
96	SC49	-773.5	1162.1
97	SC50	-864.5	1162.1
98	SC51	-955.5	1162.1
99	SC52	-1046.5	1162.1
100	SC53	-1137.5	1162.1
101	SC54	-1228.5	1162.1